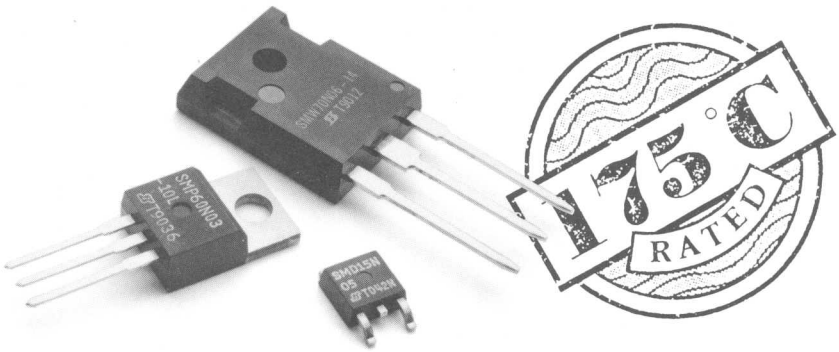
NEW POWER PRODUCTS

SiMOS 2.5

Low-Voltage,
Low On-Resistance MOSFETS



APPLICATIONS:

Solid-State Relays
Synchronous Rectifiers
DC/DC Converters
Low-Dropout Voltage Regulators
Anti-Skid Braking Systems
Motor Drives

Siliconix

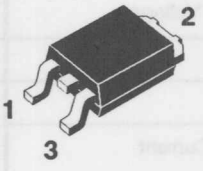
Table of Contents

Siliconix incorporated

SMD25N05-45L

N-Channel Enhancement Mode Transistor
Logic Level

D-PAK
(TO-252)



1 GATE
2 DRAIN (TAB)
3 SOURCE

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)[1]
50	0.045	25

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A = 25°C	I_D	5.0	A
	T_A = 100°C		3.1	
Pulsed Drain Current[2]		I_{DM}	100	
Avalanche Current		I_{AR}	25	
Repetitive Avalanche Energy[3]	L = 0.1 mH	E_{AR}	31	mJ
Power Dissipation	T_C = 25°C	P_D	50	W
	T_A = 25°C		2	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		2.5	K/W
Junction-to-Ambient	R_{thJA}		60	
Case-to-Sink	R_{thCS}	1.0		

[1]Calculated rating for T_C = 25°C for comparison purposes only. This cannot be used as continuous rating (see absolute maximum ratings and Figures 9, 10, 11).
[2]Pulse width limited by maximum junction temperature.
[3]Duty cycle ≤ 1%.

Preliminary

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.8	1.0	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 2 V, V_{GS} = 10 V		25		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 12.5 A	0.035		0.045	Ω
		V_{GS} = 10 V, I_D = 12.5 A, T_J = 125°C	0.60		0.080	
		V_{GS} = 5 V, I_D = 12.5 A	0.045		0.070	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 12.5 A	16			S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	800			pF
Output Capacitance	C_{oss}		320			
Reverse Transfer Capacitance	C_{rss}		90			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 25 A	27			nC
Gate-Source Charge[2]	Q_{gs}		6			
Gate-Drain Charge[2]	Q_{gd}		8			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 1 Ω, I_D ≃ 25 A, V_{GEN} = 10 V, R_G = 7.5 Ω	8		20	ns
Rise Time[2]	t_r		20		40	
Turn-Off Delay Time[2]	$t_{d(off)}$		35		60	
Fall Time[2]	t_f		20		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				25	A
Pulsed Current[3]	I_{SM}				100	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V	1.0		1.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	90			ns
Peak Reverse Recovery Current	$I_{RM(REC)}$					A
Reverse Recovery Charge	Q_{rr}					µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

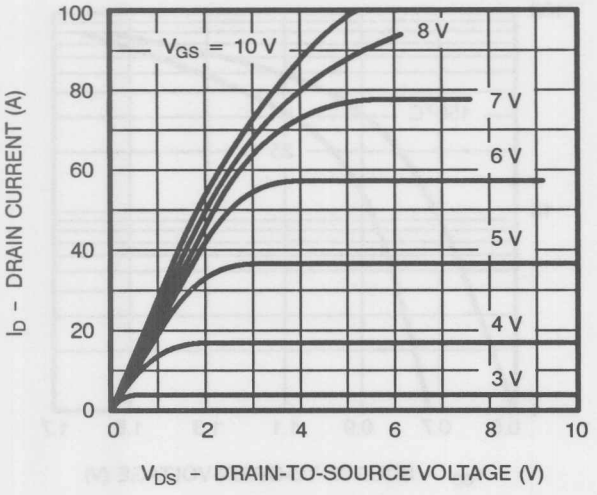


Figure 2. Transfer Characteristics

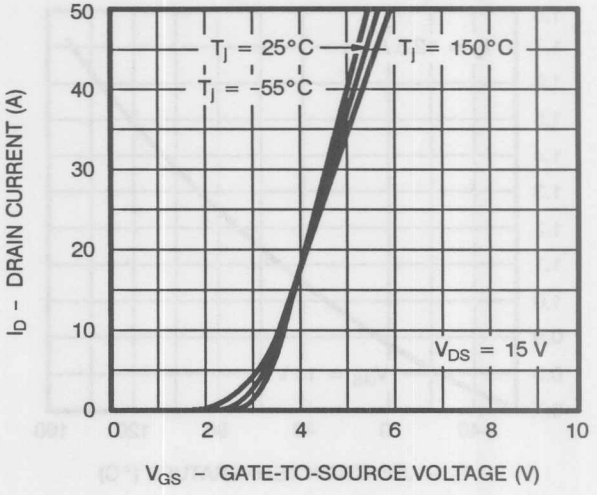


Figure 3. Transconductance

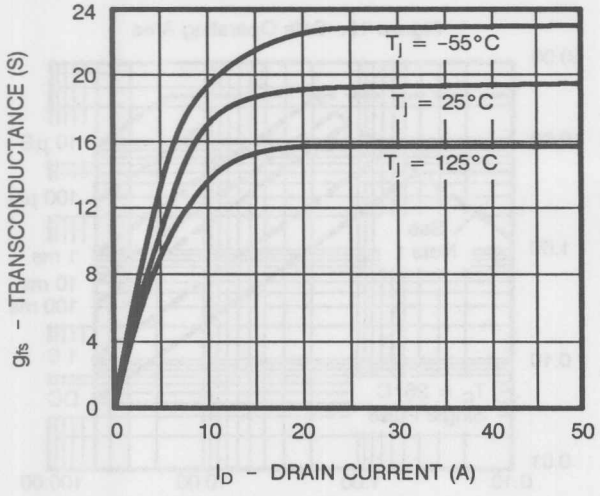


Figure 4. On-Resistance

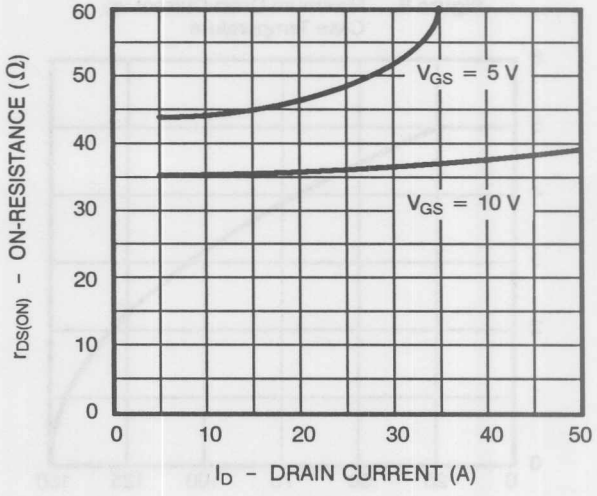


Figure 5. Capacitance

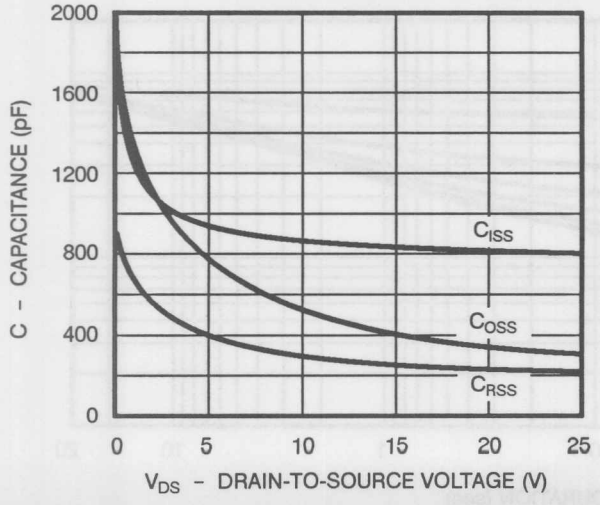
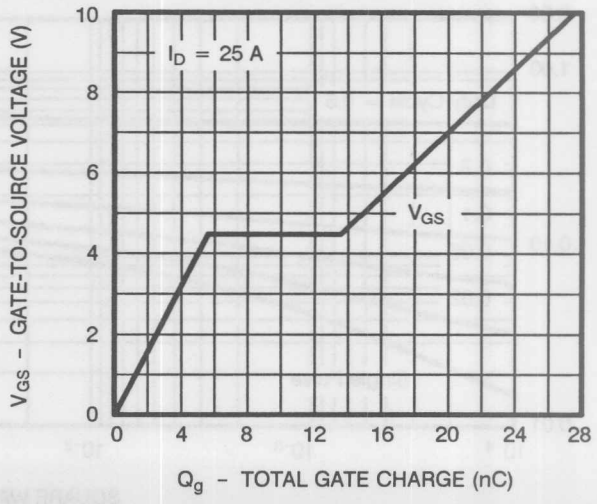


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

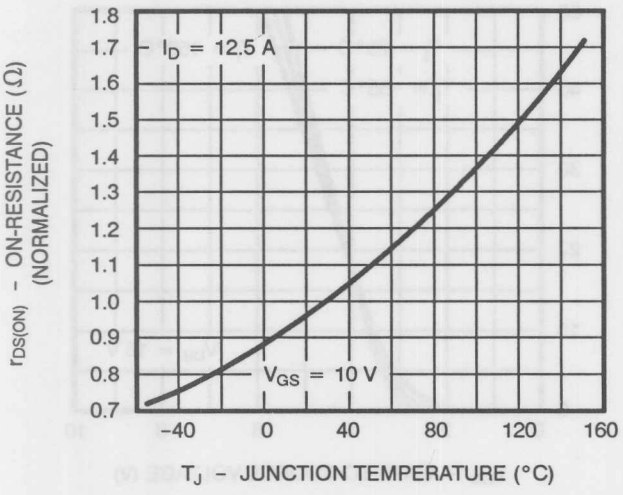
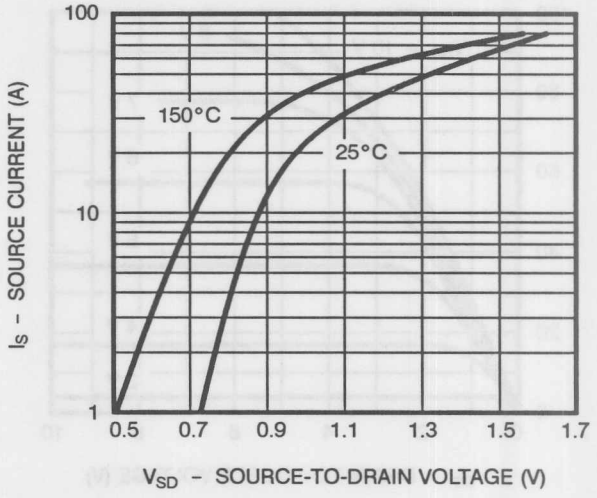


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

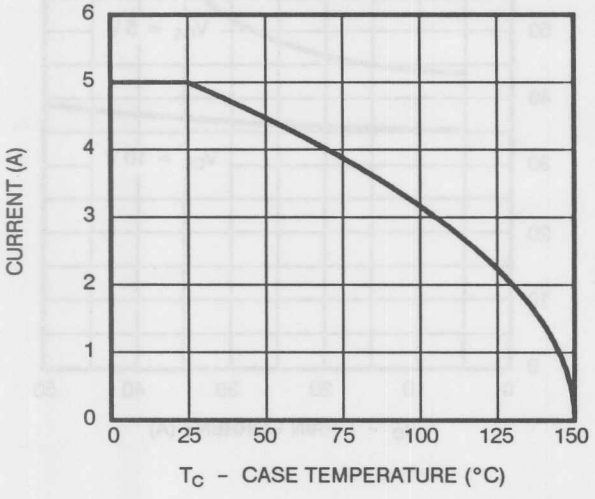
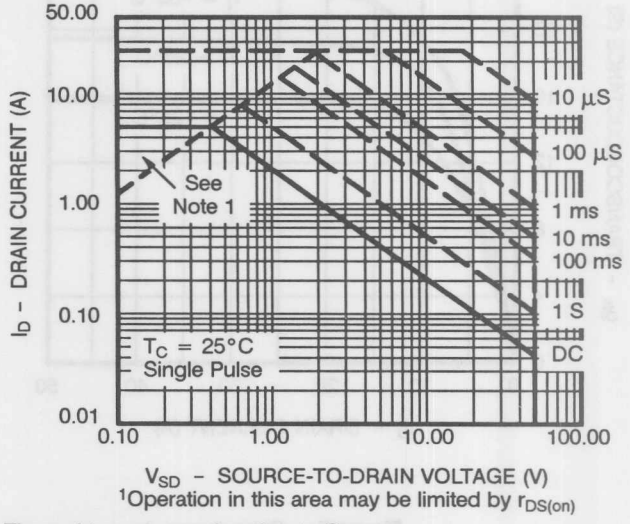
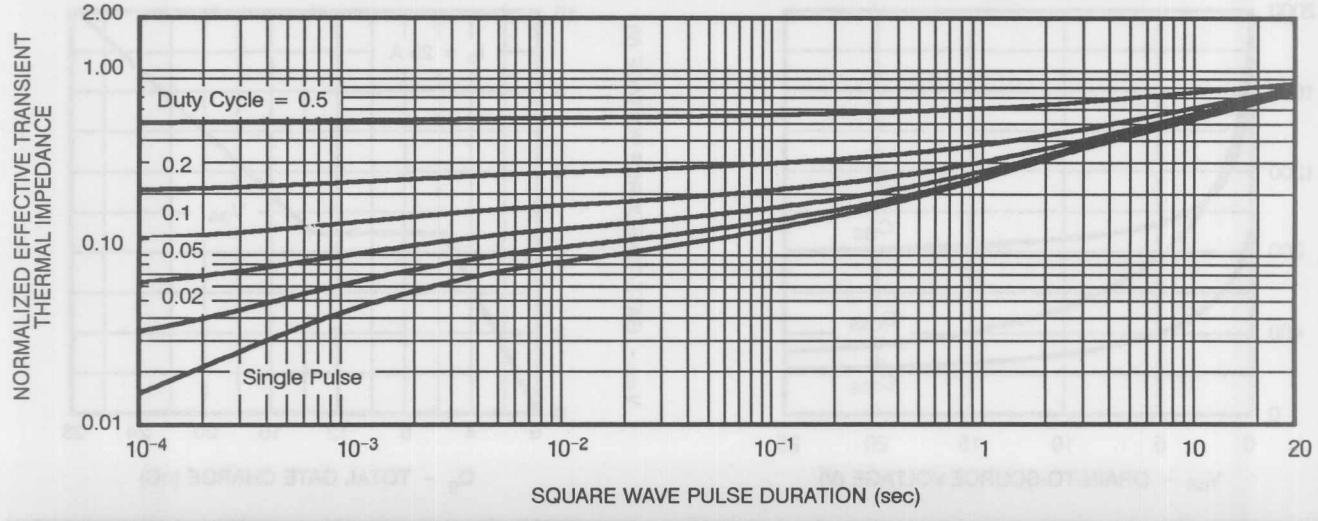


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

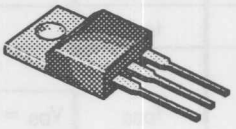


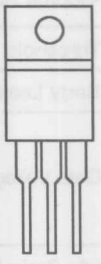
Siliconix incorporated

SMP25N05-45L

N-Channel Enhancement Mode Transistor
175°C Maximum Junction Temperature
Logic Level

TO-220AB **TOP VIEW**





1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
50	0.045	25

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	25	A
	T_C = 100°C		16	
Pulsed Drain Current[1]		I_{DM}	100	
Avalanche Current (See Figure 9)		I_{AR}	25	
Repetitive Avalanche Energy[2]	L = 0.05 mH	E_{AR}	31	mJ
Power Dissipation	T_C = 25°C	P_D	70	W
	T_C = 100°C		36	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		2.08	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle ≤ 1%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.8	1.0	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 2 V, V_{GS} = 10 V		25		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 12.5 A	0.035		0.045	Ω
		V_{GS} = 10 V, I_D = 12.5 A, T_J = 125°C	0.060		0.080	
		V_{GS} = 5 V, I_D = 12.5 A	0.045		0.070	
		V_{GS} = 10 V, I_D = 12.5 A, T_J = 175°C	0.062		0.085	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 12.5 A	16			S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	800			pF
Output Capacitance	C_{oss}		320			
Reverse Transfer Capacitance	C_{rss}		90			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 25 A	27			nC
Gate-Source Charge[2]	Q_{gs}		6			
Gate-Drain Charge[2]	Q_{gd}		8			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 1 Ω, I_D ≃ 25 A, V_{GEN} = 10 V, R_G = 7.5 Ω	8		20	ns
Rise Time[2]	t_r		20		40	
Turn-Off Delay Time[2]	$t_{d(off)}$		35		60	
Fall Time[2]	t_f		20		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				25	A
Pulsed Current[3]	I_{SM}				100	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V	1.0		1.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	90			ns
Peak Reverse Recovery Time	$I_{RM(REC)}$					A
Reverse Recovery Charge	Q_{rr}					µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

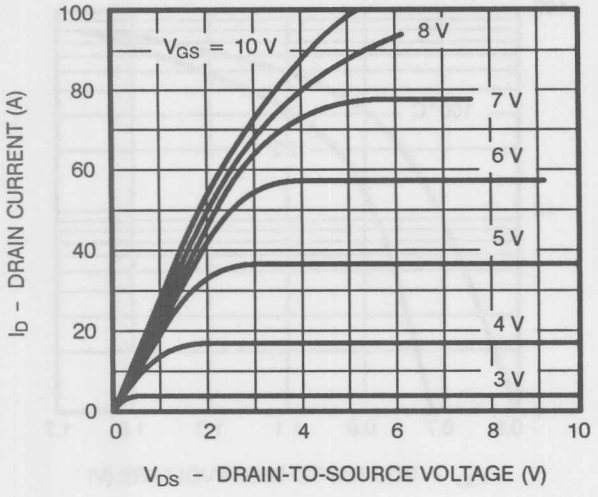


Figure 2. Transfer Characteristics

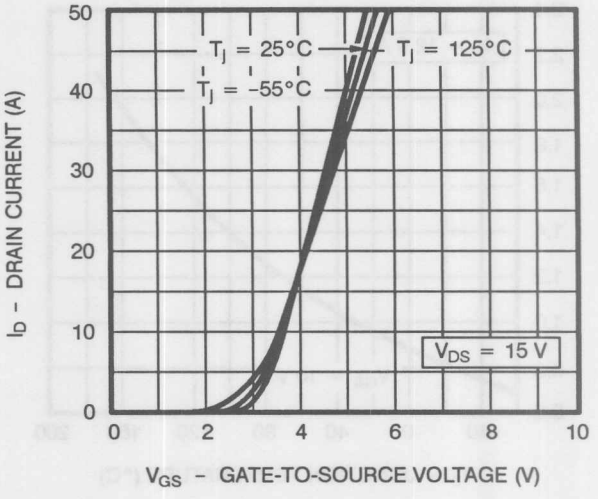


Figure 3. Transconductance

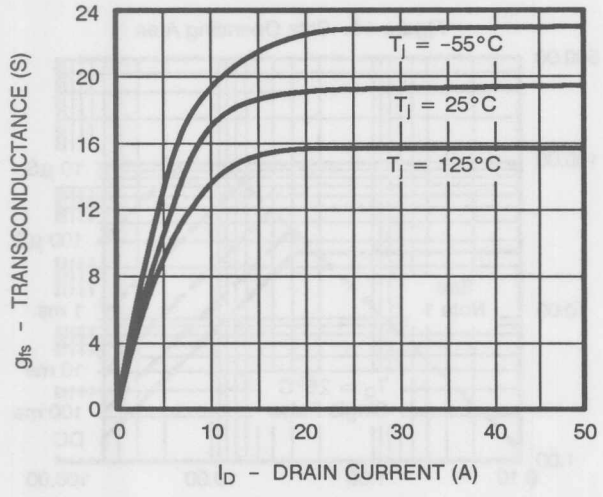


Figure 4. On-Resistance

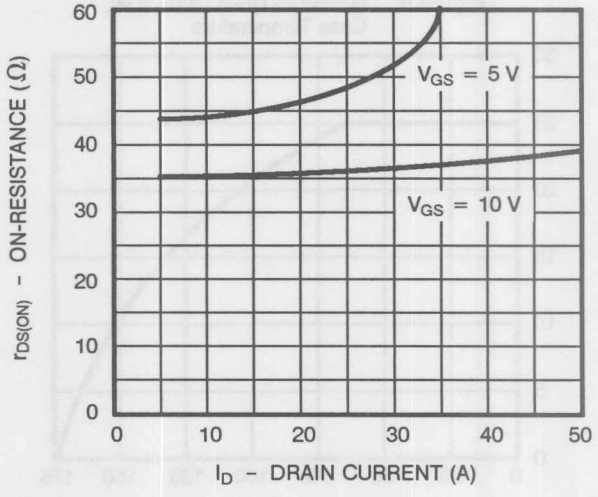


Figure 5. Capacitance

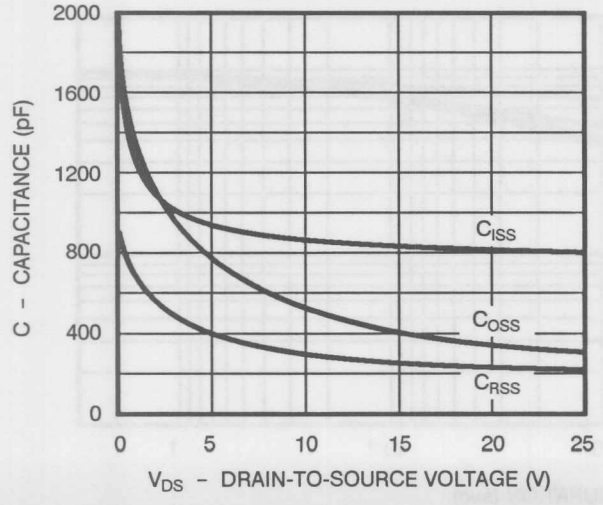
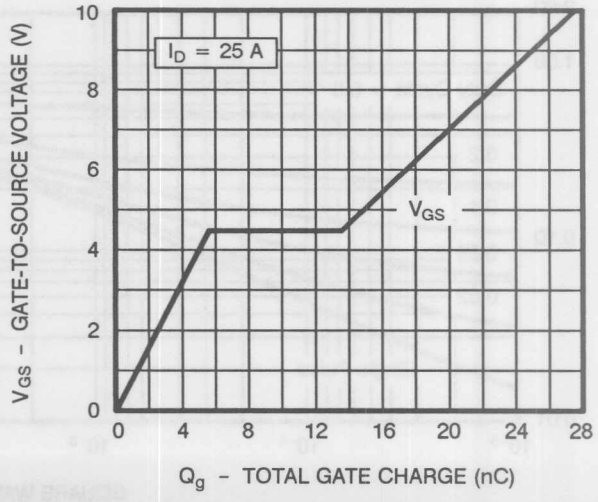


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

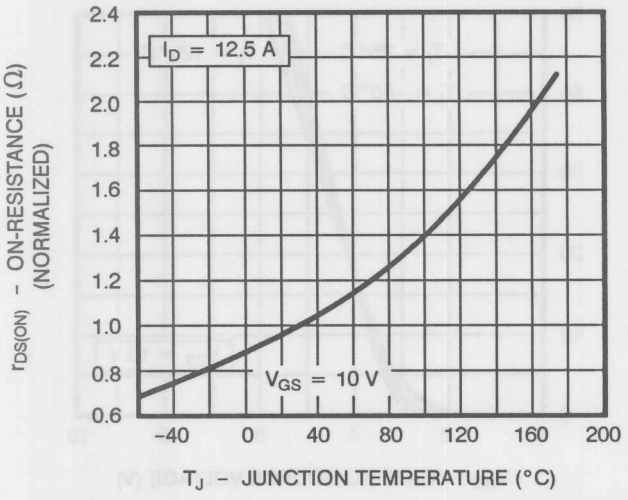
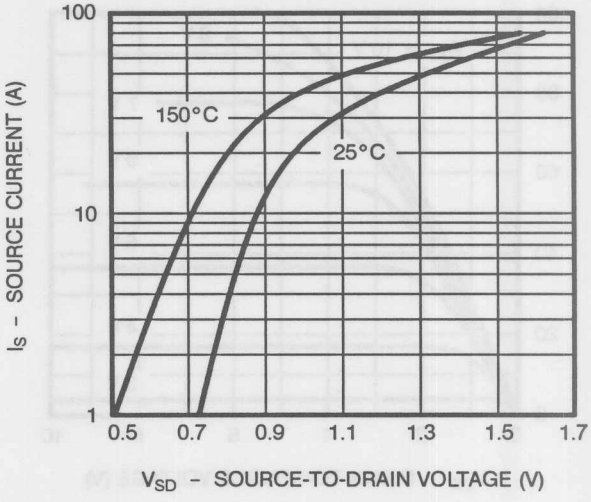


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

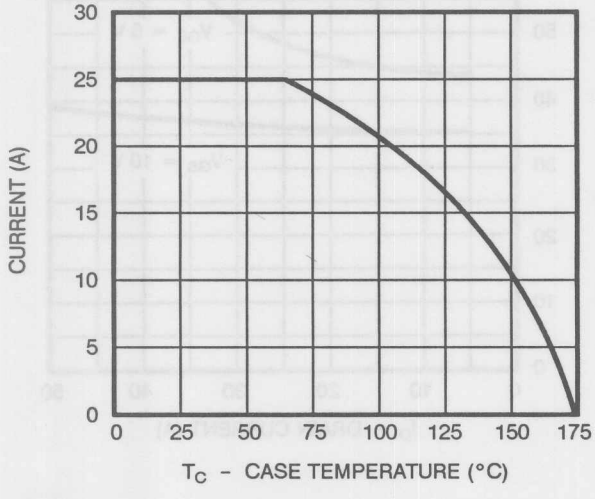
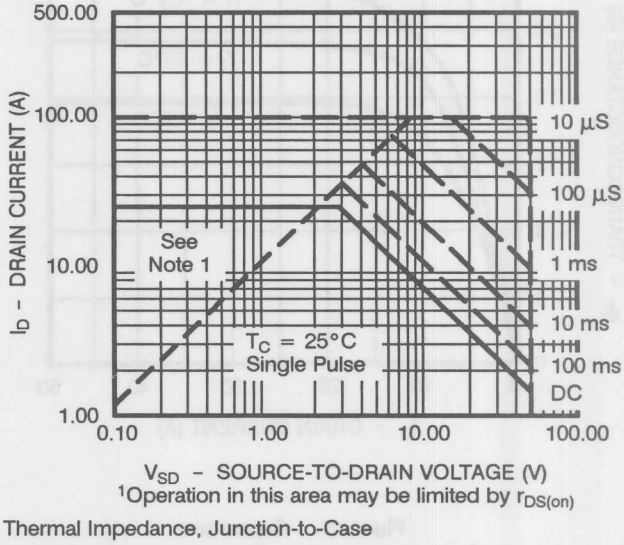
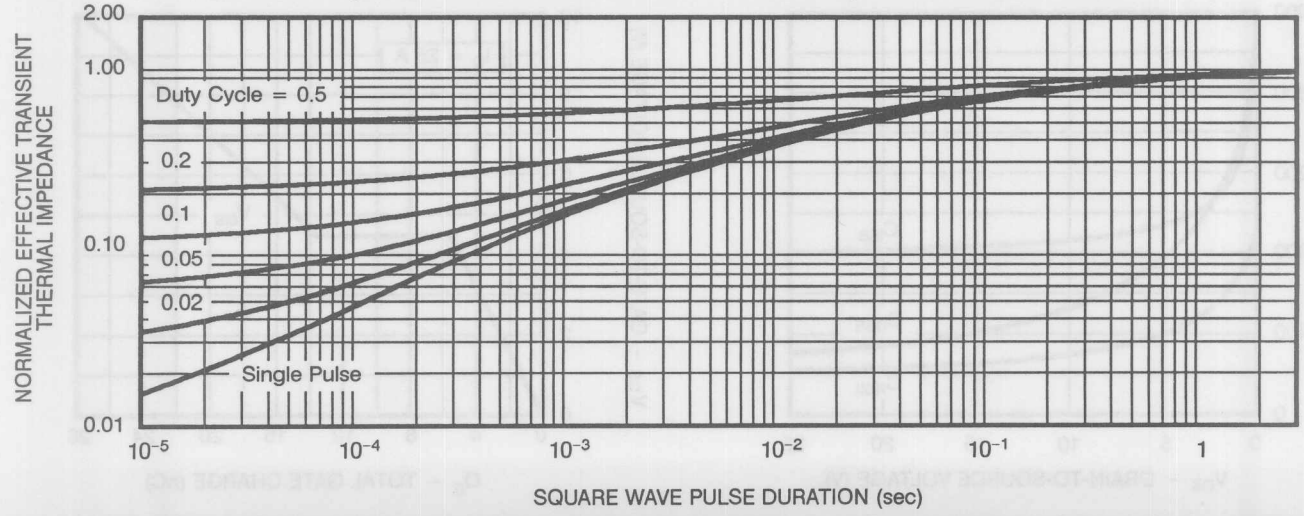


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

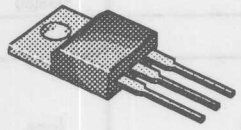
SMP50N06-25

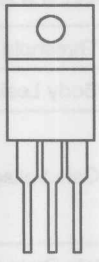
N-Channel Enhancement Mode Transistor
175°C Maximum Junction Temperature[1]
25 milli ohm $r_{DS(ON)}$

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	0.025	46

TO-220AB **TOP VIEW**





1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	46	A
	T_C = 100°C		32	
Pulsed Drain Current[2]		I_{DM}	200	
Avalanche Current		I_{AR}	46	
Avalanche Energy	L = 0.1 mH	E_{AS}	125	mJ
Repetitive Avalanche Energy[3]	L = 0.05 mH	E_{AR}	62.5	
Power Dissipation	T_C = 25°C	P_D	105	W
	T_C = 100°C		53	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 175[1]	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.4	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Applies to datecode 9118 and higher.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[3]Duty cycle ≤ 1%.

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		50		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 25 A	0.020		0.025	Ω
		V_{GS} = 10 V, I_D = 25 A, T_J = 125°C	0.033		0.042	
		V_{GS} = 10 V, I_D = 25 A, T_J = 175°C	0.043		0.0525	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 25 A	20			S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2000			pF
Output Capacitance	C_{oss}		570			
Reverse Transfer Capacitance	C_{rss}		120			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 50 A	55		80	nC
Gate-Source Charge[2]	Q_{gs}		9		15	
Gate-Drain Charge[2]	Q_{gd}		24		40	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.6 Ω, I_D ≃ 50 A, V_{GEN} = 10 V, R_G = 2.5 Ω	15		30	ns
Rise Time[2]	t_r		20		35	
Turn-Off Delay Time[2]	$t_{d(off)}$		40		65	
Fall Time[2]	t_f		15		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				46	A
Pulsed Current[3]	I_{SM}				200	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	130			ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		10			A
Reverse Recovery Charge	Q_{rr}		0.7			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

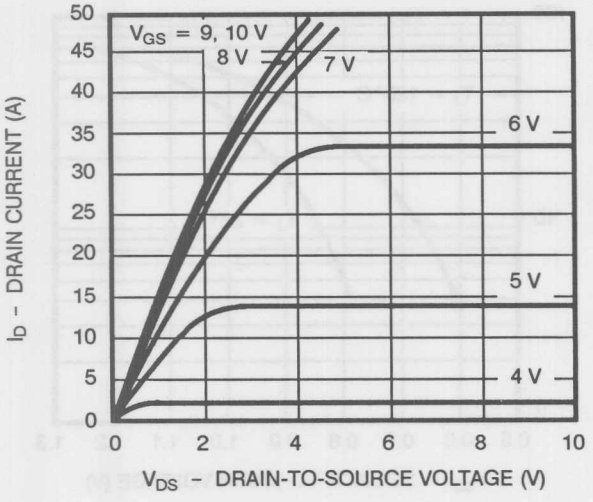


Figure 2. Transfer Characteristics

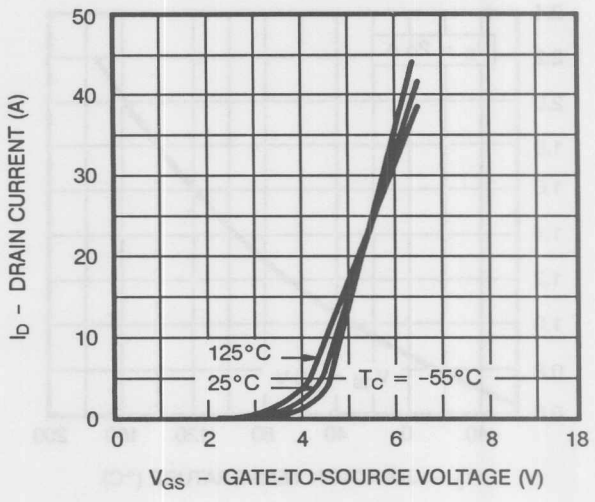


Figure 3. Transconductance

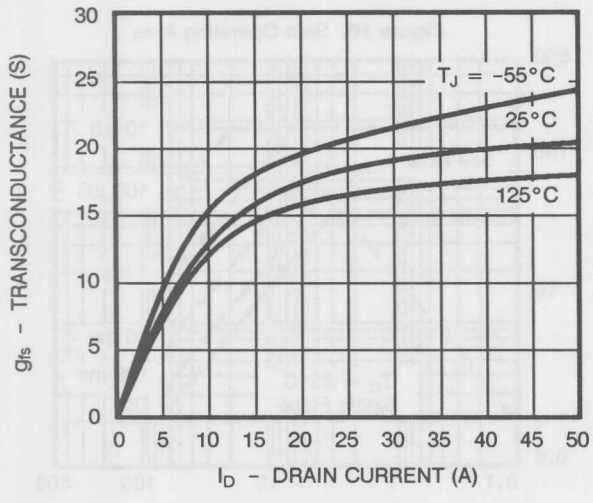


Figure 4. On-Resistance

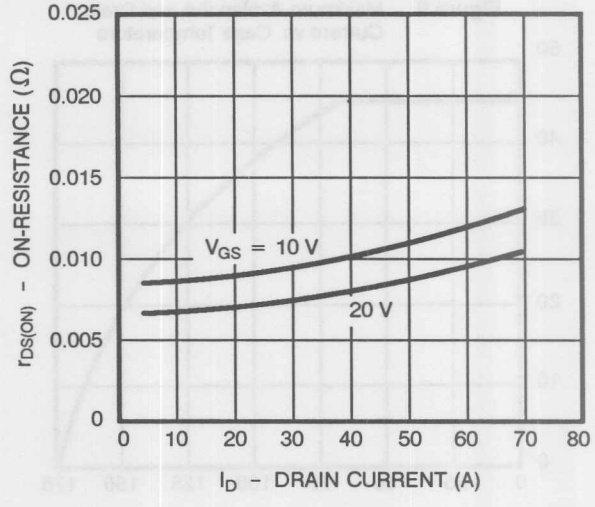


Figure 5. Capacitance

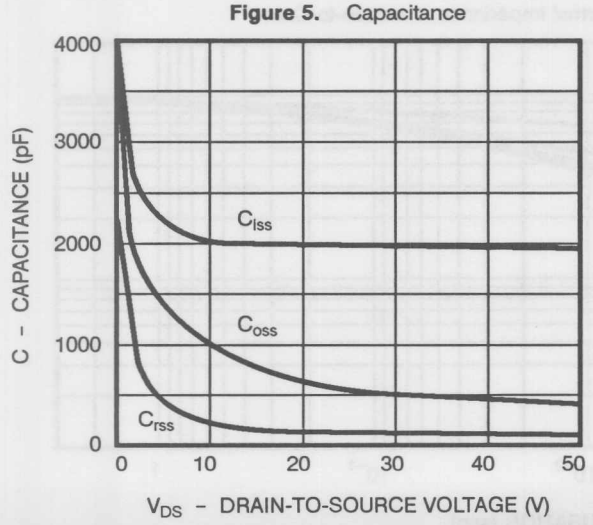
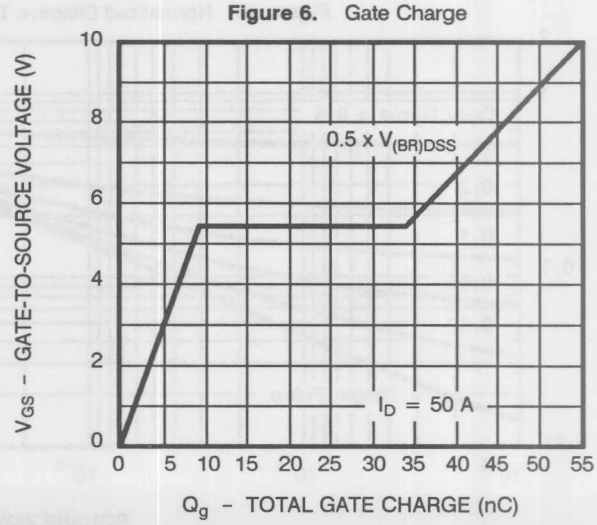


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

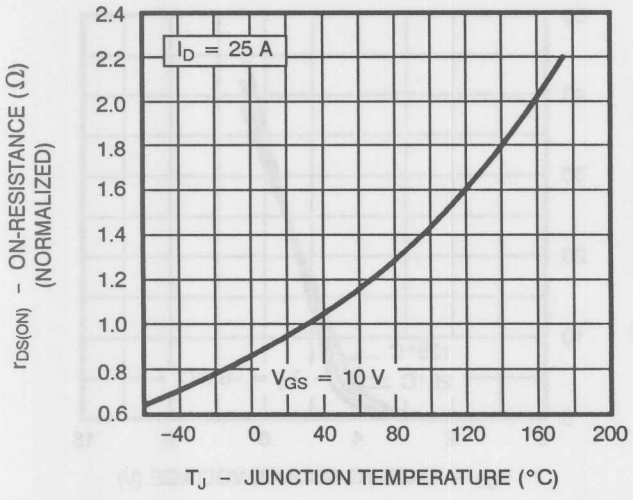
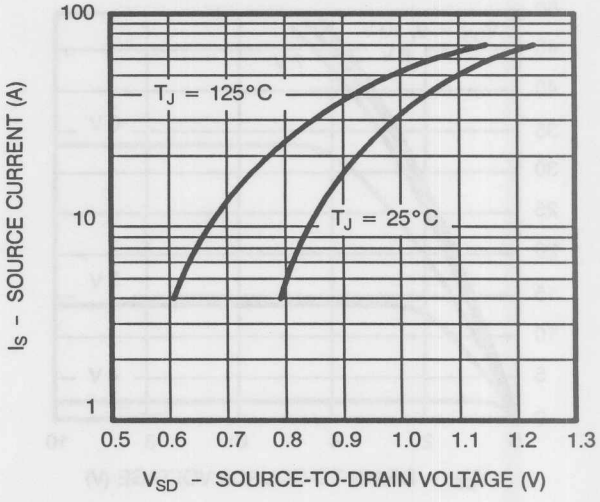


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

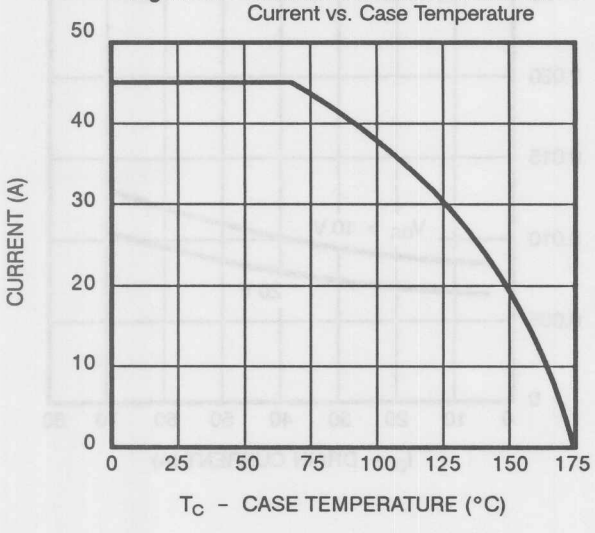
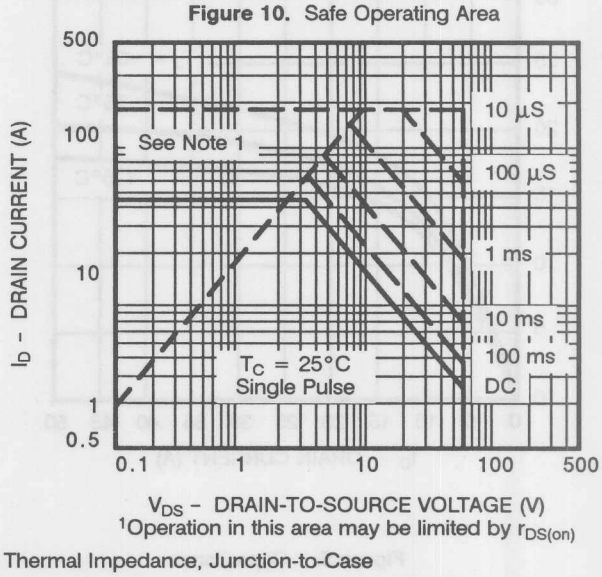
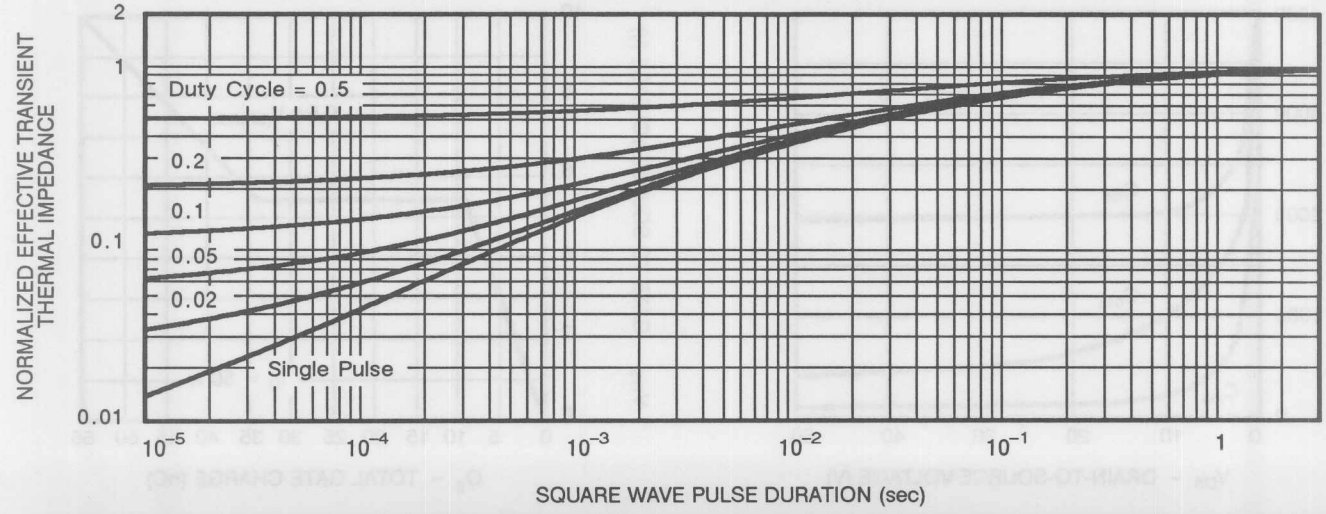


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

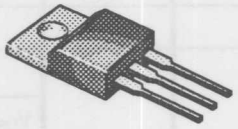
SMP60N03-10L

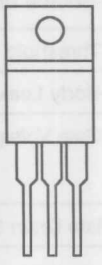
N-Channel Enhancement Mode Transistor
10 milli ohm $r_{DS(ON)}$ Logic Level

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
30	0.010	60

TO-220AB **TOP VIEW**





1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		51	
Pulsed Drain Current[1]		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.1 mH	E_{AS}	180	mJ
Repetitive Avalanche Energy[2]	L = 0.05 mH	E_{AR}	90	
Power Dissipation	T_C = 25°C	P_D	105	W
	T_C = 100°C		42	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.2	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		0.8	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		60		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 30 A	0.007		0.010	Ω
		V_{GS} = 5 V, I_D = 30 A	0.010		0.015	
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C	0.009		0.014	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	45			S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2600			pF
Output Capacitance	C_{oss}		1500			
Reverse Transfer Capacitance	C_{rss}		750			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A	100		120	nC
Gate-Source Charge[2]	Q_{gs}		10		15	
Gate-Drain Charge[2]	Q_{gd}		45		75	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω I_D ≃ 30 A, V_{GEN} = 10 V, R_G = 2.5 Ω	14		30	ns
Rise Time[2]	t_r		25		50	
Turn-Off Delay Time[2]	$t_{d(off)}$		65		100	
Fall Time[2]	t_f		45		80	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current[3]	I_{SM}				240	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.6	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	160			ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		13			A
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

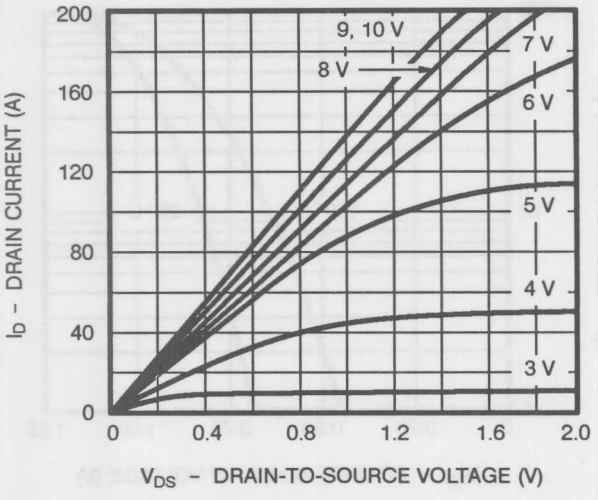


Figure 2. Transfer Characteristics

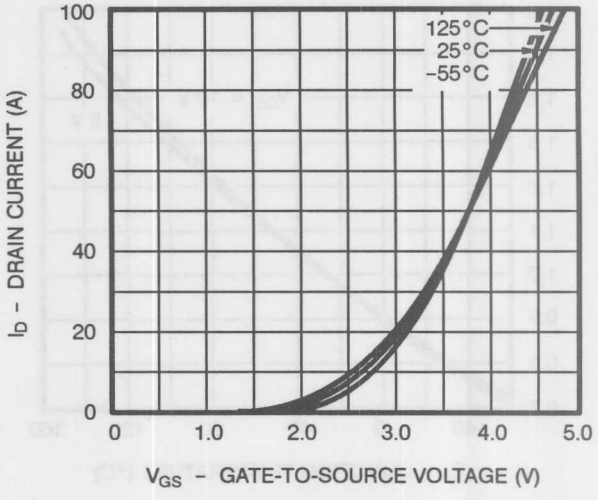


Figure 3. Transconductance

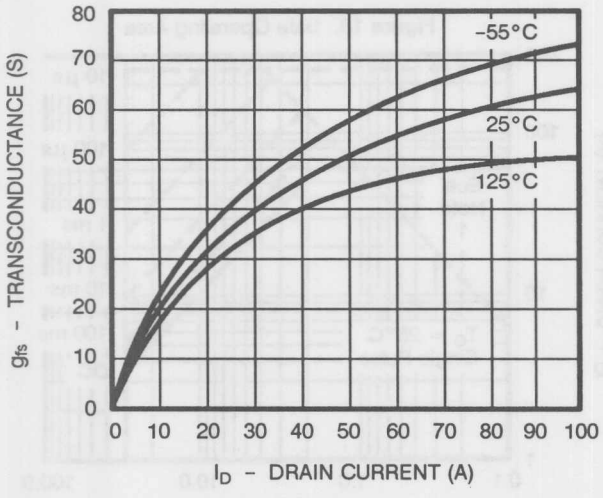


Figure 4. On-Resistance

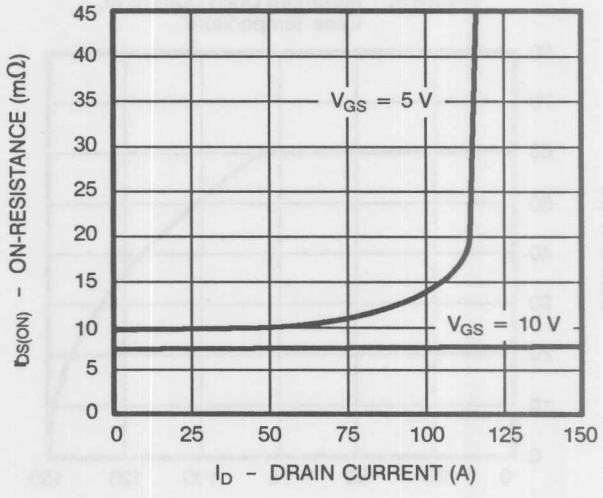


Figure 5. Capacitance

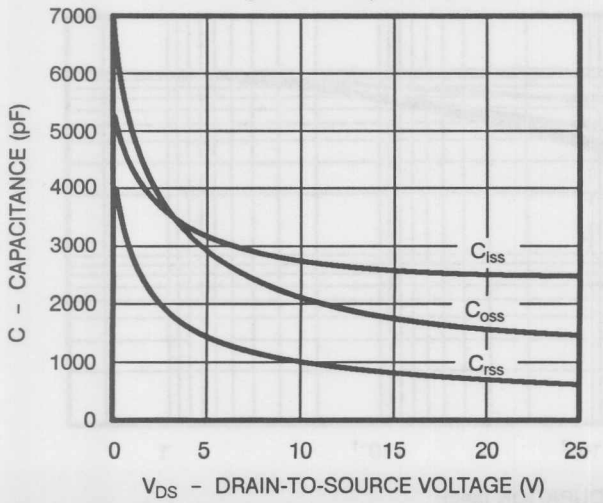


Figure 6. Gate Charge

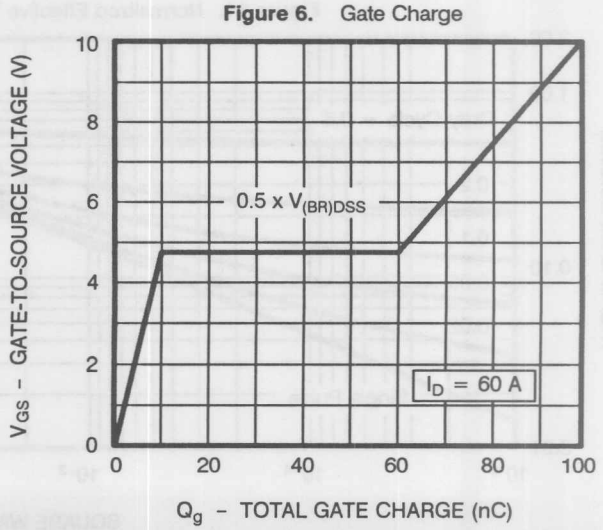


Figure 7. On-Resistance vs. Junction Temperature

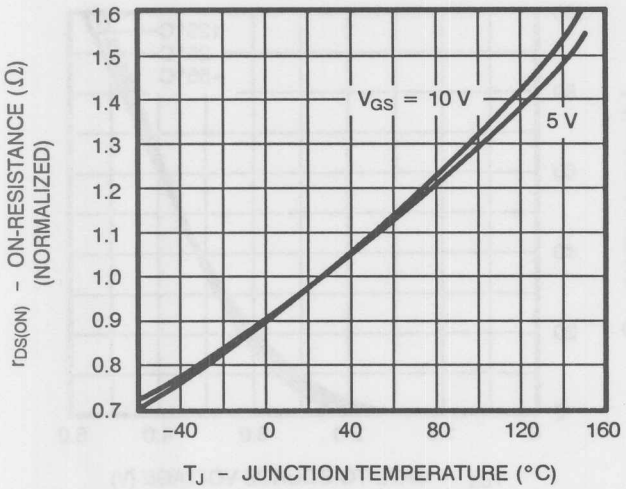
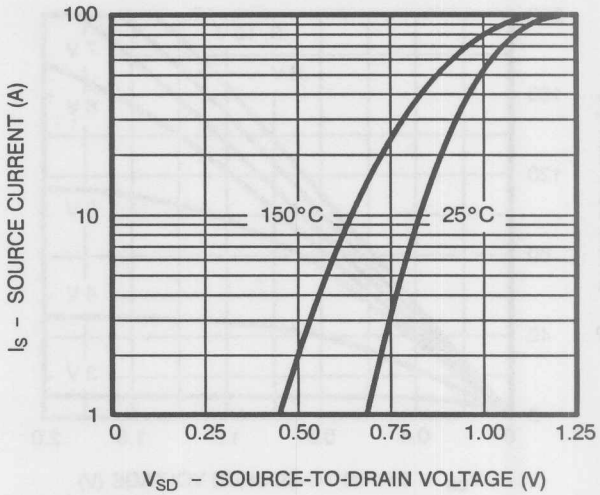


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

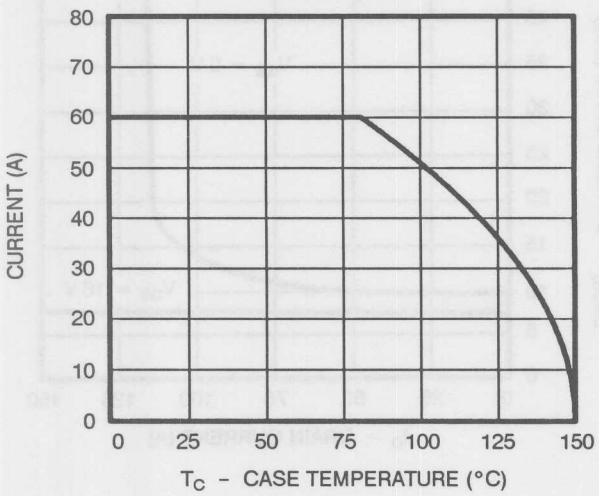
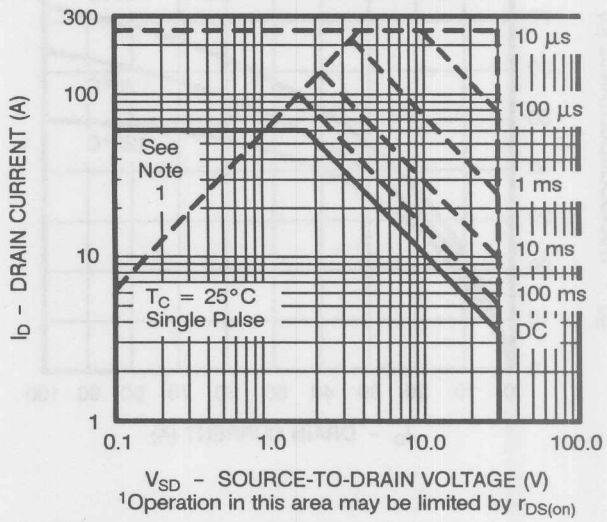
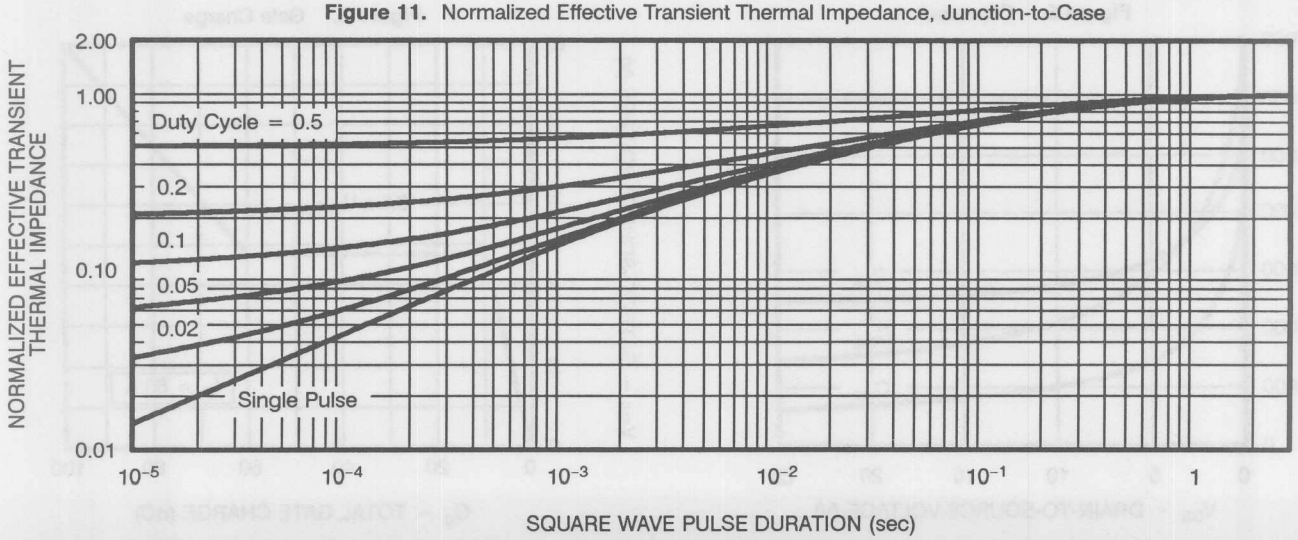


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

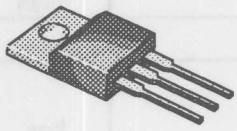
SMP60N06-14

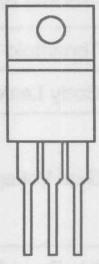
N-Channel Enhancement Mode Transistor
175°C Maximum Junction Temperature[1]

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	0.014	60[2]

TO-220AB **TOP VIEW**





1 2 3

1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60[2]	A
	T_C = 100°C		50	
Pulsed Drain Current[3]		I_{DM}	240	
Avalanche Current[4]		I_{AR}	60	
Repetitive Avalanche Energy	L = 0.1 mH	E_{AR}	180	mJ
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		75	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Applies to datecode 9118 and higher.
[2]Package limited.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[4]Duty cycle ≤ 1%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	3.0	2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		60		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 30 A	0.012		0.014	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C	0.020		0.023	
		V_{GS} = 10 V, I_D = 30 A, T_J = 175°C	0.025		0.028	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	48	30		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	3450			pF
Output Capacitance	C_{oss}		1000			
Reverse Transfer Capacitance	C_{rss}		230			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A	95		130	nC
Gate-Source Charge[2]	Q_{gs}		20			
Gate-Drain Charge[2]	Q_{gd}		45			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.47 Ω, I_D ≃ 60 A, V_{GEN} = 10 V, R_G = 2.5 Ω	15		30	ns
Rise Time[2]	t_r		130		180	
Turn-Off Delay Time[2]	$t_{d(off)}$		50		100	
Fall Time[2]	t_f		20		50	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current[3]	I_{SM}				240	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V	1.0		1.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	130		200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		9			A
Reverse Recovery Charge	Q_{rr}		0.6			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

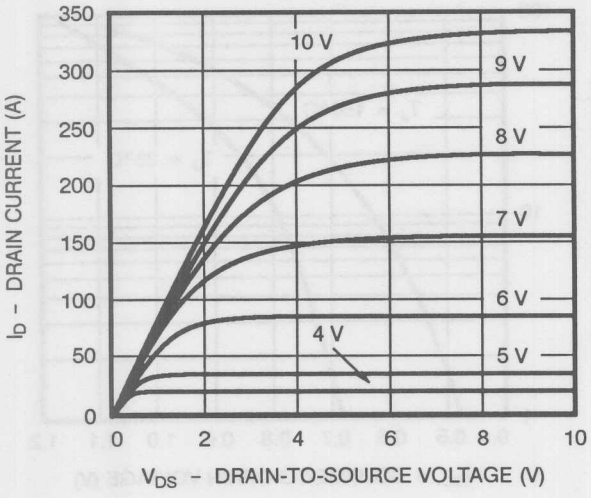


Figure 2. Transfer Characteristics

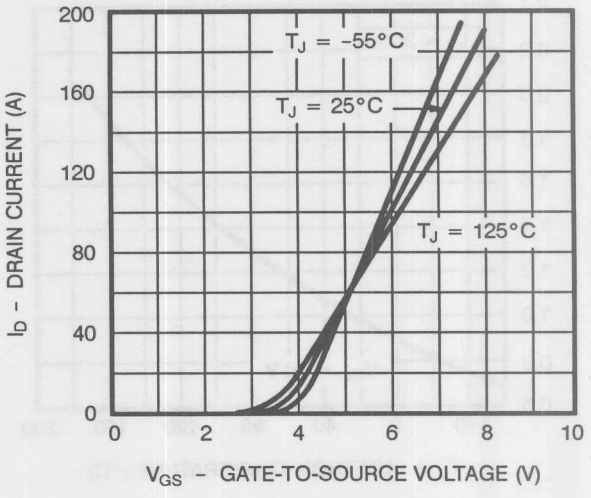


Figure 3. Transconductance

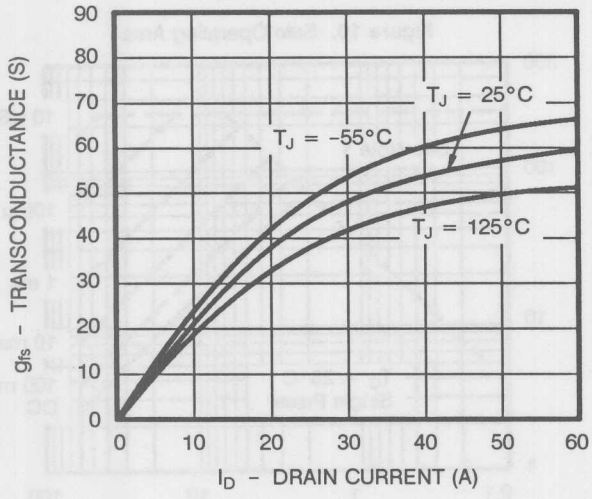


Figure 4. On-Resistance

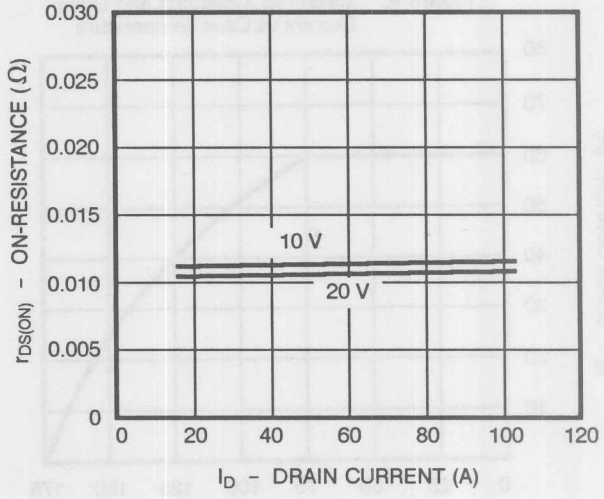


Figure 5. Capacitance

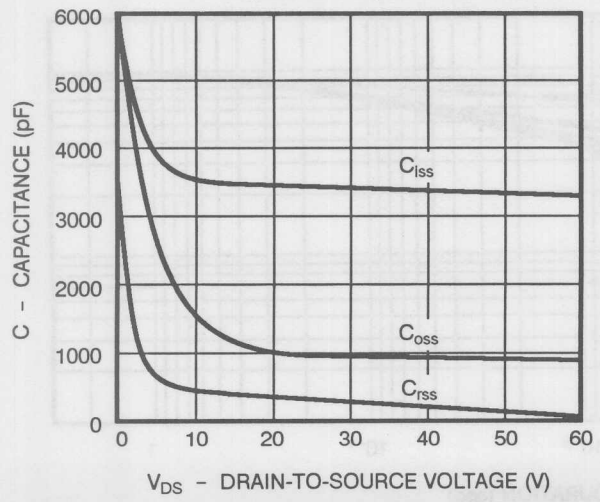
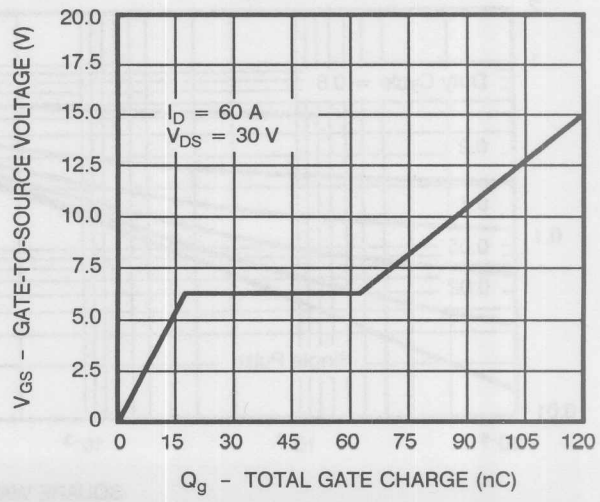


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

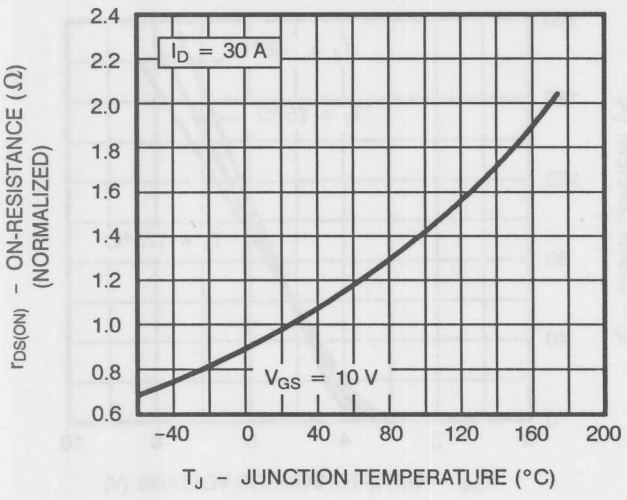
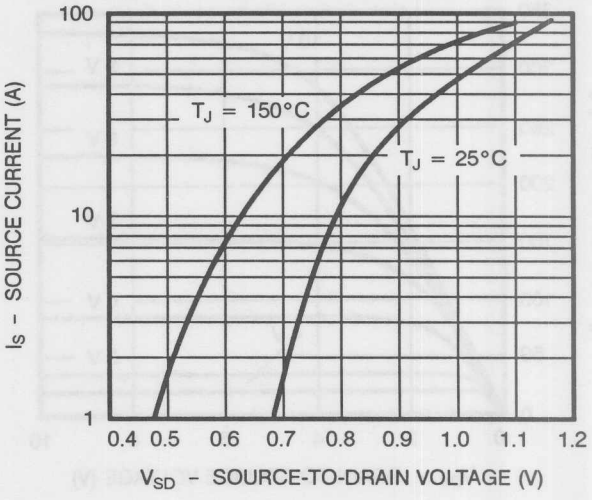


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs.Case Temperature

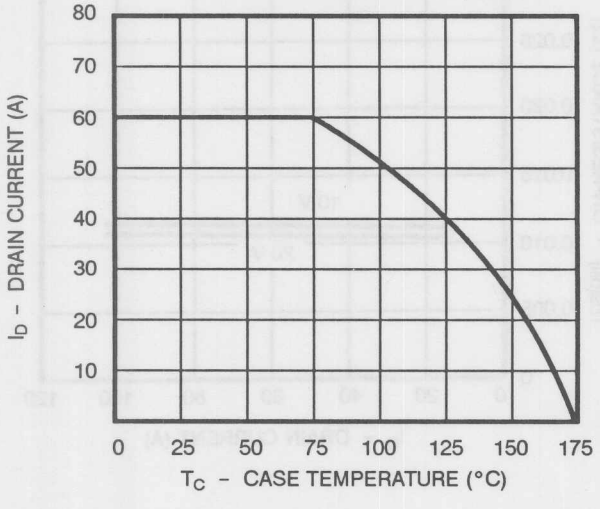
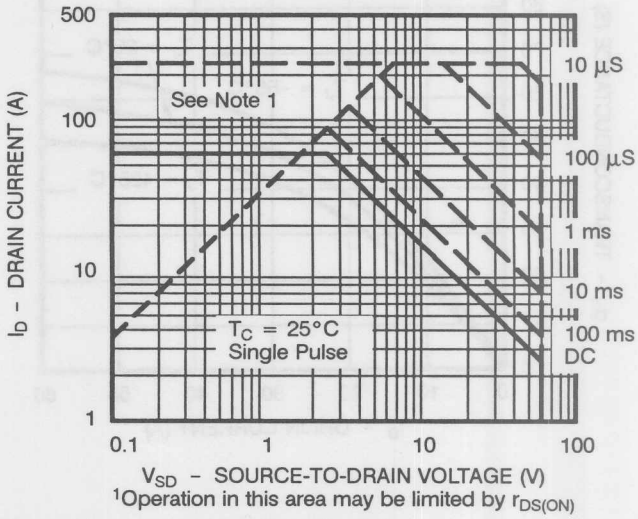
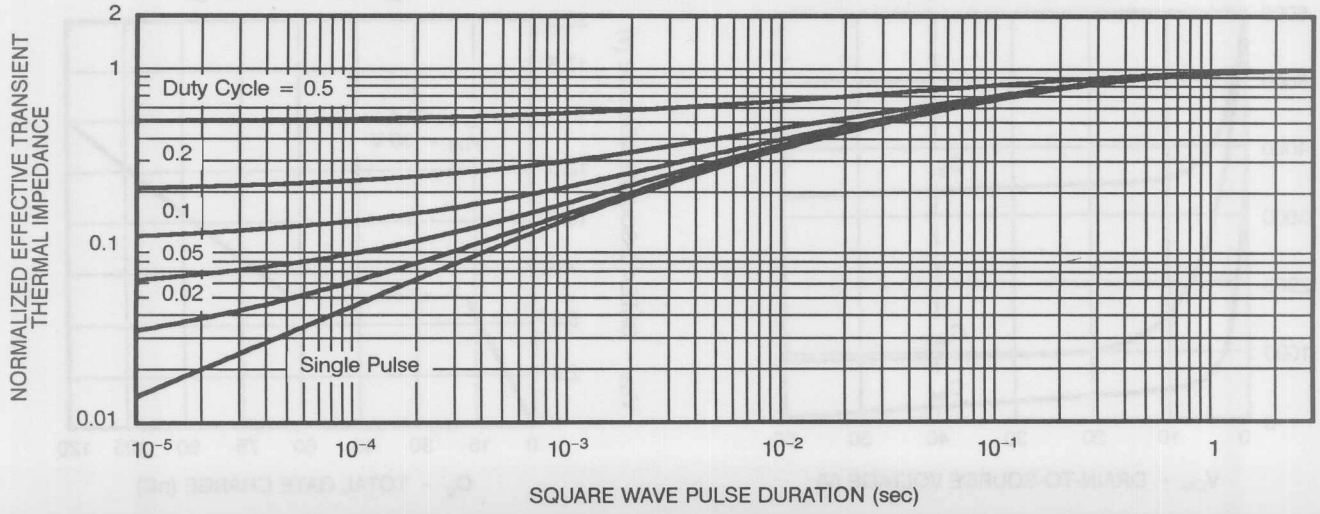


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(ON)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

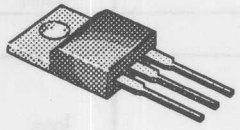
SMP60N06-18

N-Channel Enhancement Mode Transistor
175°C Maximum Junction Temperature[1]
18 milli ohm $r_{DS(ON)}$

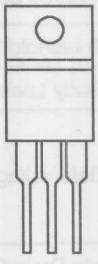
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	0.018	60

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		41	
Pulsed Drain Current[2]		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.1 mH	E_{AS}	180	mJ
Repetitive Avalanche Energy[3]	L = 0.05 mH	E_{AR}	90	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		62	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.2	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Applies to datecode 9118 and higher.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[3]Duty cycle ≤ 1%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		60		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 30 A	0.013		0.018	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C	0.023		0.030	
		V_{GS} = 10 V, I_D = 30 A, T_J = 175°C	0.026		0.036	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	45			S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2600			pF
Output Capacitance	C_{oss}		800			
Reverse Transfer Capacitance	C_{rss}		200			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A	85		100	nC
Gate-Source Charge[2]	Q_{gs}		15		20	
Gate-Drain Charge[2]	Q_{gd}		35		50	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω, I_D ≃ 30 A, V_{GEN} = 10 V, R_G = 2.5 Ω	15		30	ns
Rise Time[2]	t_r		20		35	
Turn-Off Delay Time[2]	$t_{d(off)}$		50		65	
Fall Time[2]	t_f		15		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current[3]	I_{SM}				240	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	160			ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		13			A
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

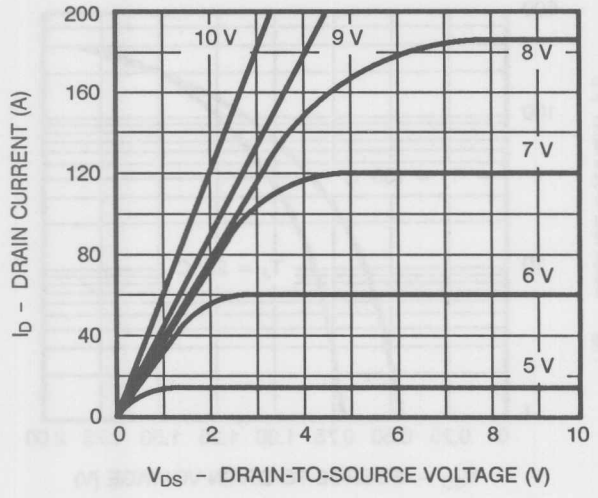


Figure 2. Transfer Characteristics

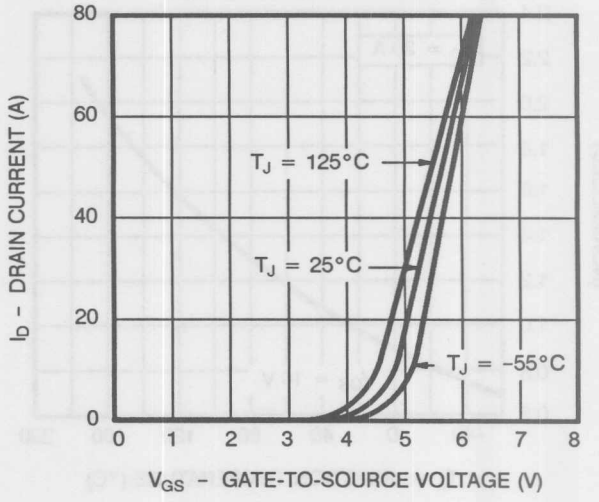


Figure 3. Transconductance

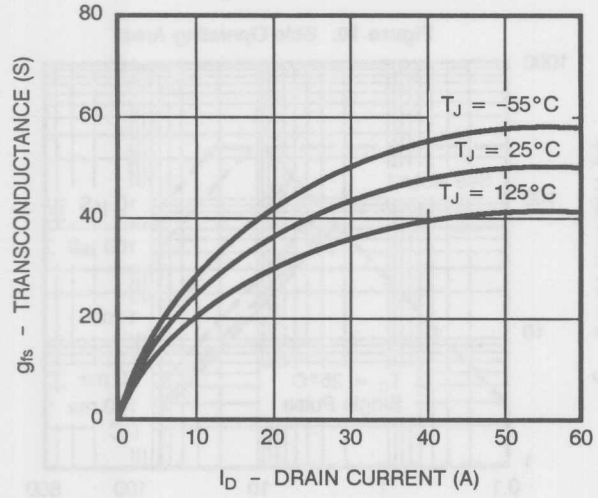


Figure 4. On-Resistance

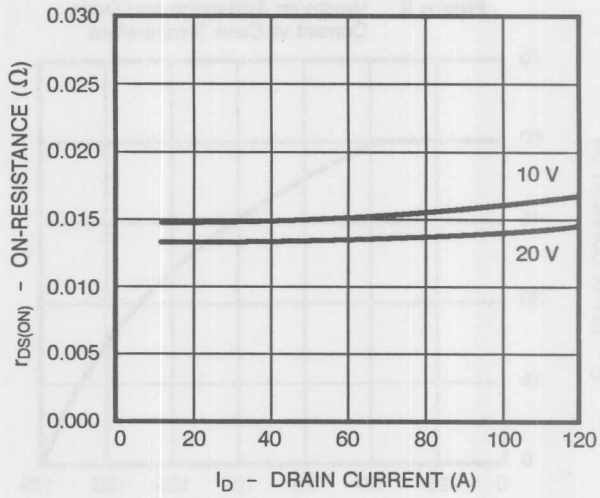


Figure 5. Capacitance

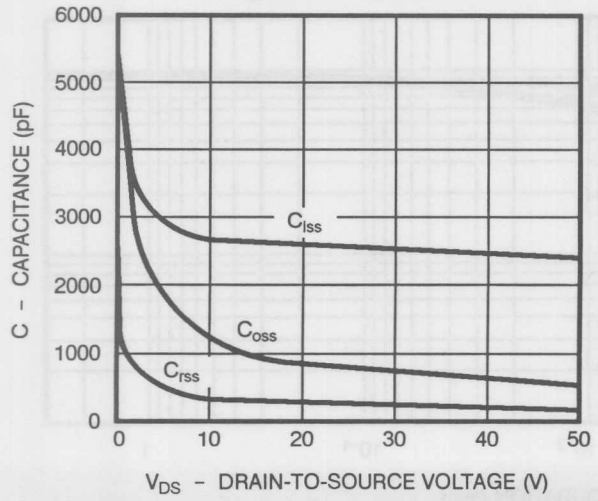
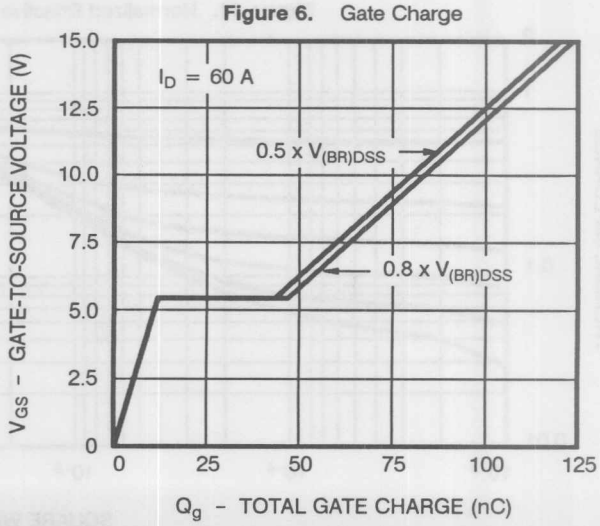


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

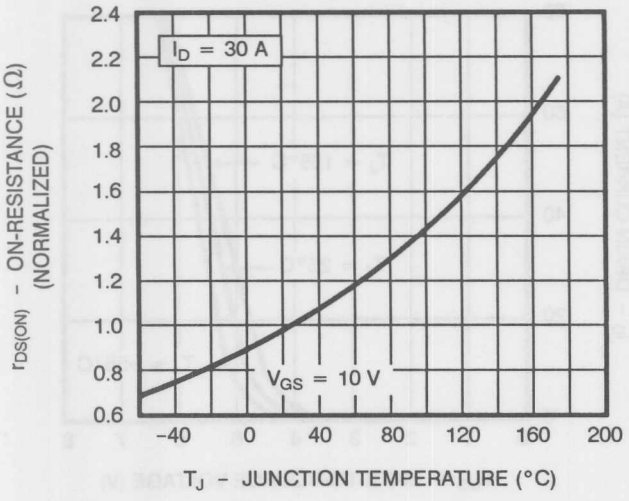
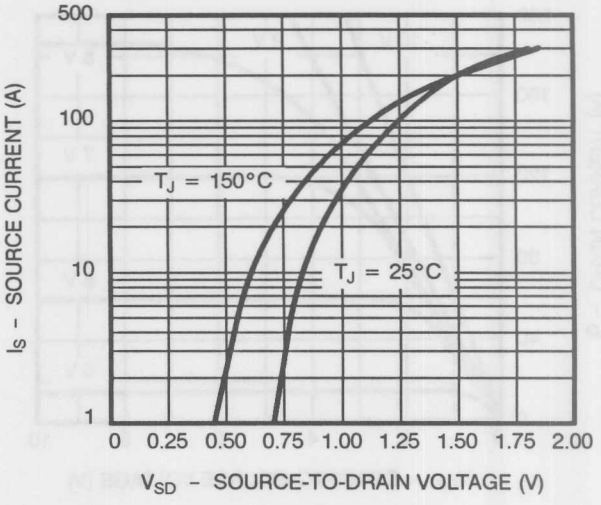


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs.Case Temperature

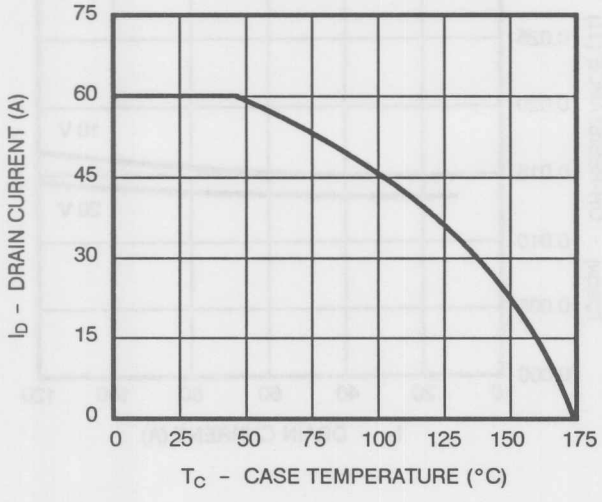
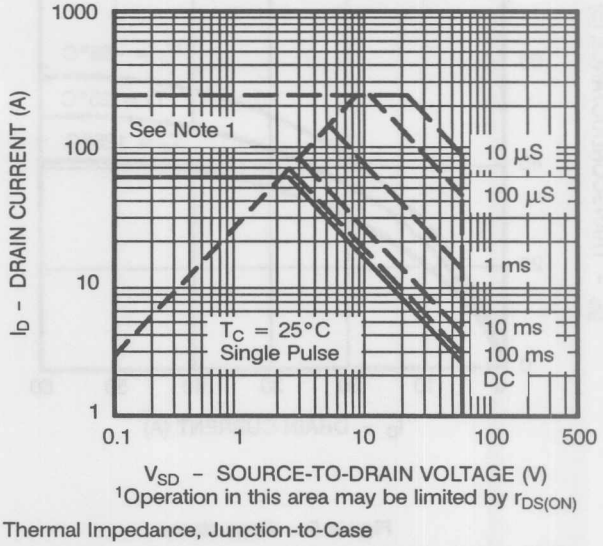
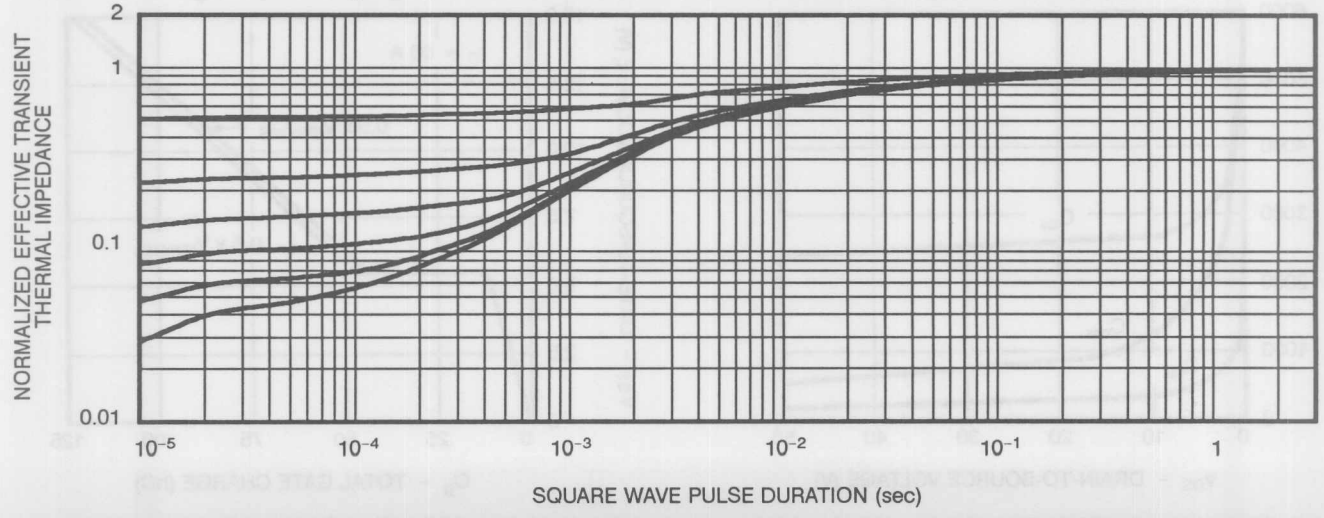


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(ON)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

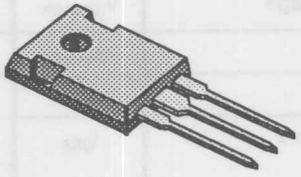


Siliconix incorporated

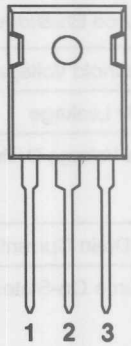
SMW60N06-18

N-Channel Enhancement Mode Transistor
18 milli ohm $r_{DS(ON)}$

TO-247 AD



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	0.018	60

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		40	
Pulsed Drain Current[1]		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.1 mH	E_{AS}	180	mJ
Repetitive Avalanche Energy[2]	L = 0.05 mH	E_{AR}	90	
Power Dissipation	T_C = 25°C	P_D	105	W
	T_C = 100°C		42	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		40	
Case-to-Sink	R_{thCS}	0.35		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		60		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 30 A	0.013		0.018	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C	0.023		0.030	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	45	15		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2600			pF
Output Capacitance	C_{oss}		800			
Reverse Transfer Capacitance	C_{rss}		200			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A	85		100	nC
Gate-Source Charge[2]	Q_{gs}		15		20	
Gate-Drain Charge[2]	Q_{gd}		35		50	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω, $I_D \simeq$ 30 A, V_{GEN} = 10 V, R_G = 2.5 Ω	15		30	ns
Rise Time[2]	t_r		20		35	
Turn-Off Delay Time[2]	$t_{d(off)}$		50		65	
Fall Time[2]	t_f		15		30	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current[3]	I_{SM}				240	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	160			ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		13			A
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

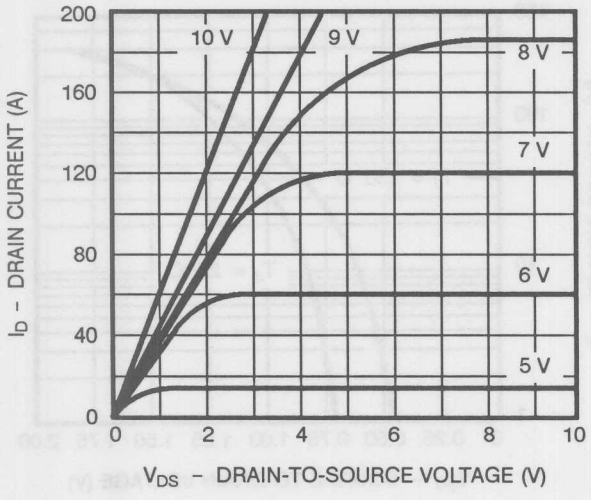


Figure 2. Transfer Characteristics

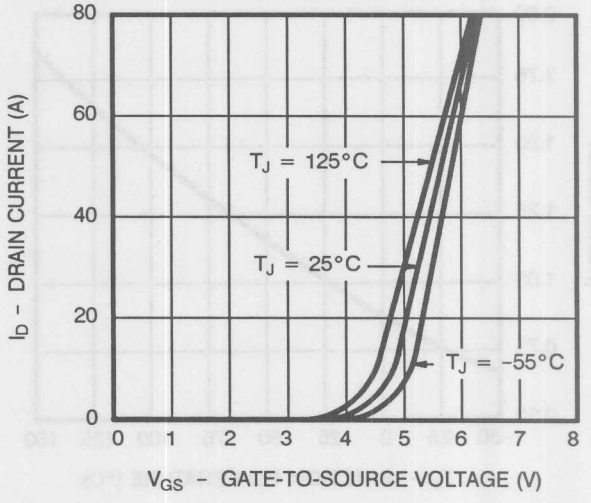


Figure 3. Transconductance

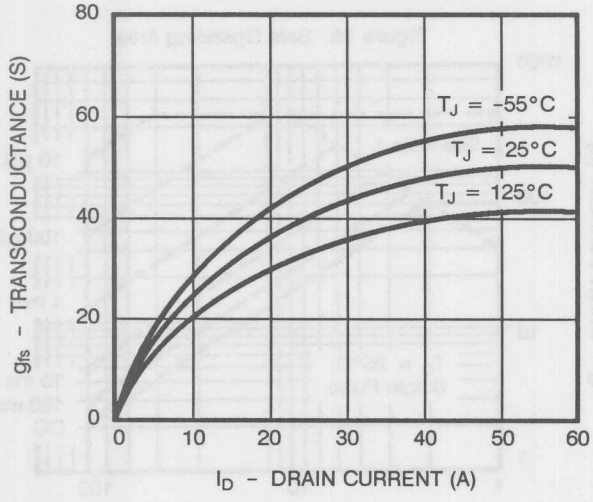


Figure 4. On-Resistance

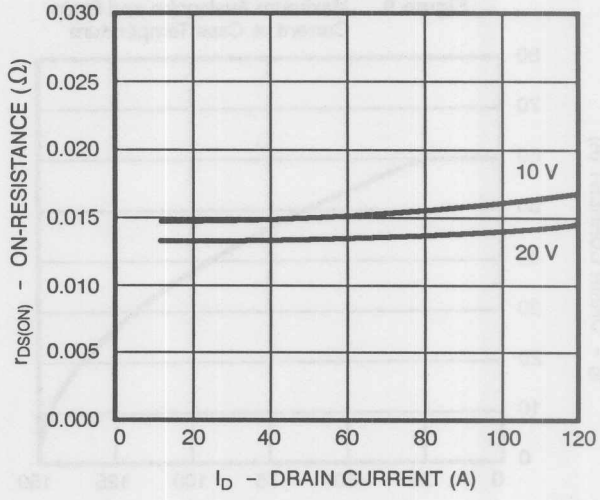


Figure 5. Capacitance

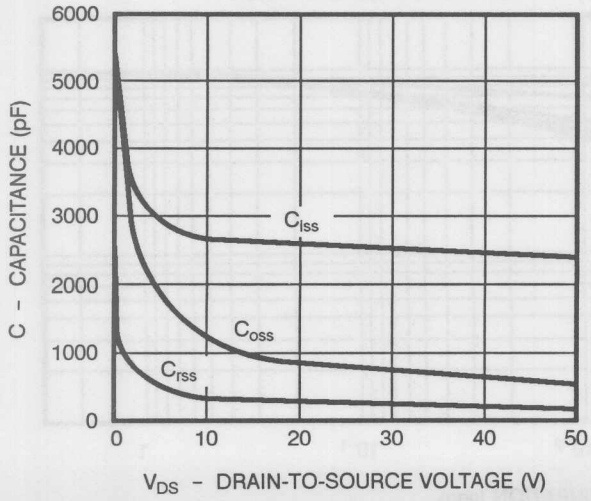
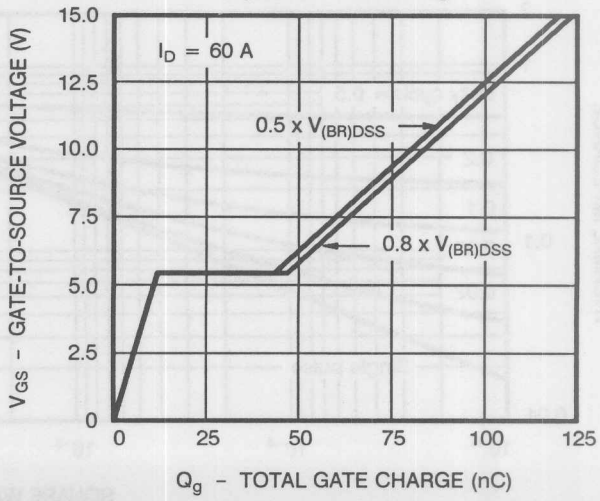


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

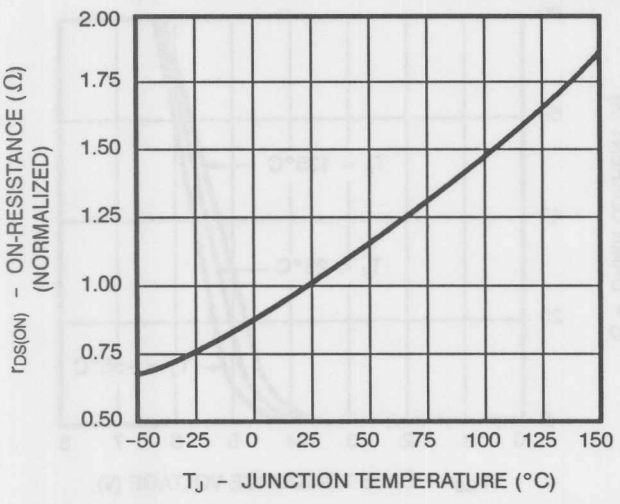
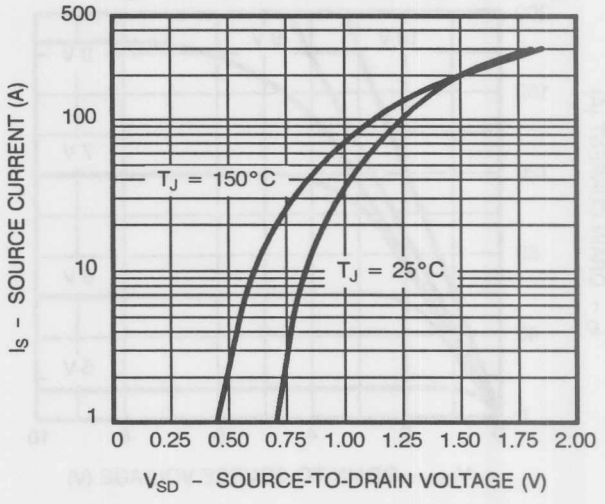


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs.Case Temperature

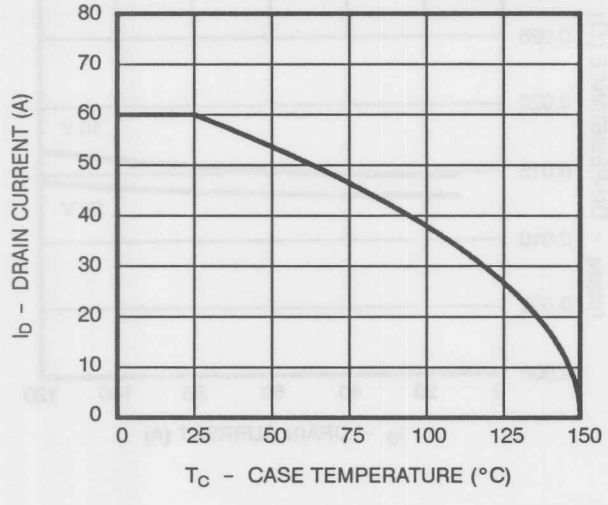
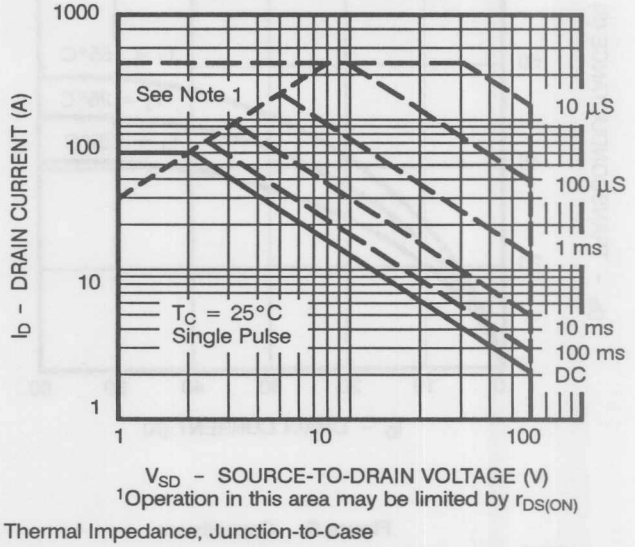
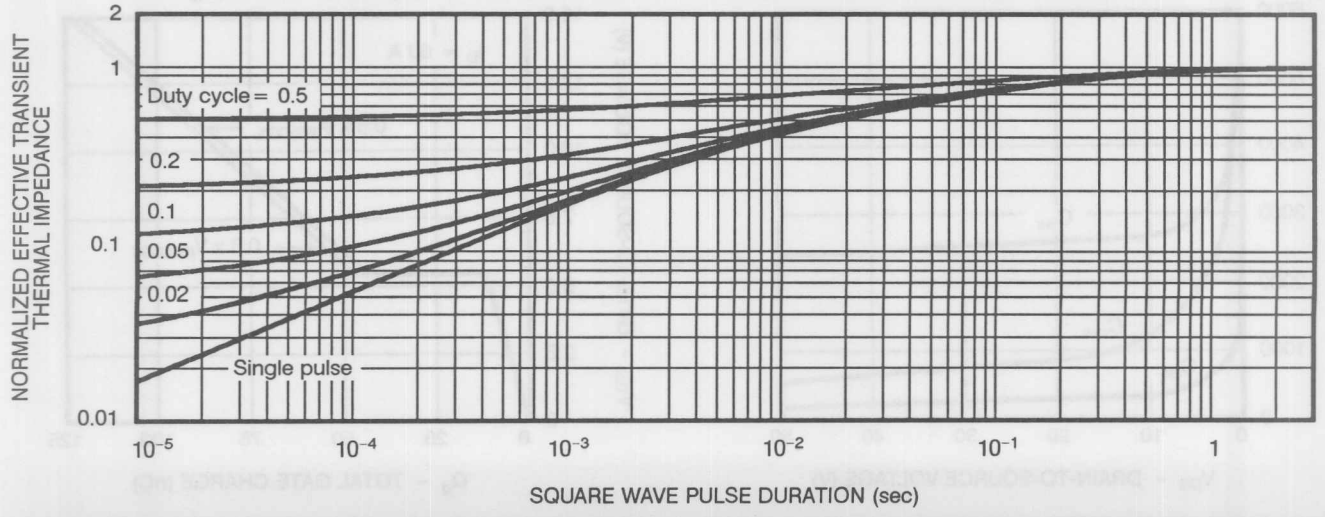


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(ON)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

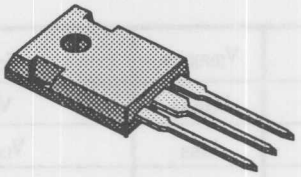


Siliconix incorporated

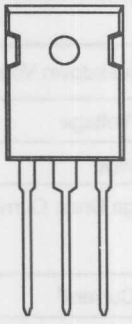
SMW70N06-14

N-Channel Enhancement Mode Transistor

TO-247 AD



TOP VIEW



1 GATE
2 DRAIN (Conneccted to TAB)
3 SOURCE

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	0.014	70[1]

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	70[1]	A
	T_C = 100°C		48	
Pulsed Drain Current[2]		I_{DM}	280	
Avalanche Current[3]		I_{AR}	70	
Repetitive Avalanche Energy	L = 0.1 mH	E_{AR}	245	mJ
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.83	K/W
Junction-to-Ambient	R_{thJA}		40	
Case-to-Sink	R_{thCS}	0.35		

[1]Package limited.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[3]Duty cycle ≤ 1%.

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	3.0	2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		80		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 35 A	0.012		0.014	Ω
		V_{GS} = 10 V, I_D = 35 A, T_J = 125°C	0.020		0.023	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 35 A	50	30		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	3450			pF
Output Capacitance	C_{oss}		1000			
Reverse Transfer Capacitance	C_{rss}		230			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 70 A	95		130	nC
Gate-Source Charge[2]	Q_{gs}		22			
Gate-Drain Charge[2]	Q_{gd}		44			
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.39 Ω, $I_D \simeq$ 70 A, V_{GEN} = 10 V, R_G = 2.5 Ω	15		30	ns
Rise Time[2]	t_r		130		180	
Turn-Off Delay Time[2]	$t_{d(off)}$		50		100	
Fall Time[2]	t_f		20		50	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				70	A
Pulsed Current[3]	I_{SM}				280	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V	1.0		1.8	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	130		200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		9			A
Reverse Recovery Charge	Q_{rr}		0.6			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

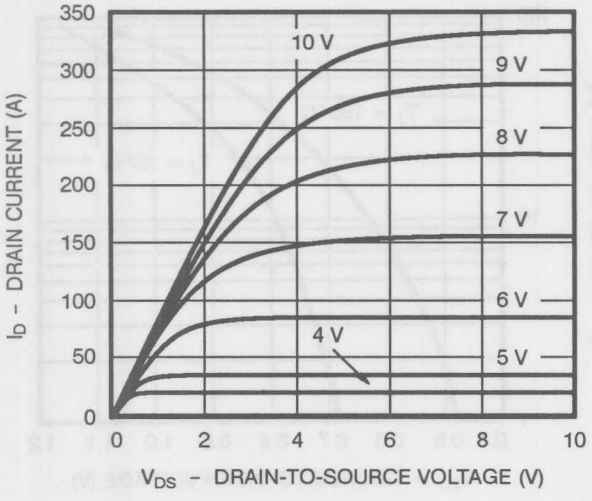


Figure 2. Transfer Characteristics

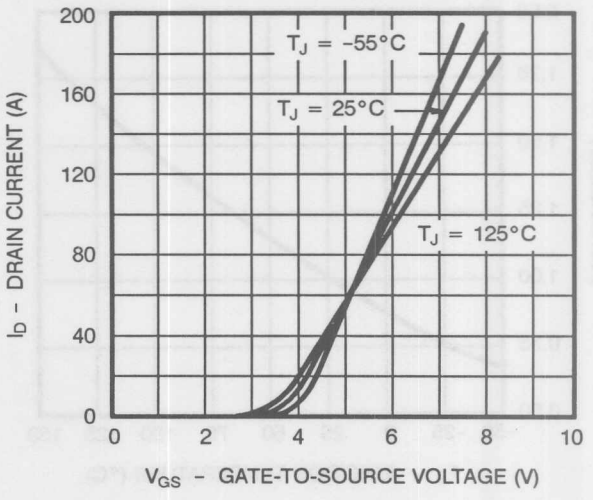


Figure 3. Transconductance

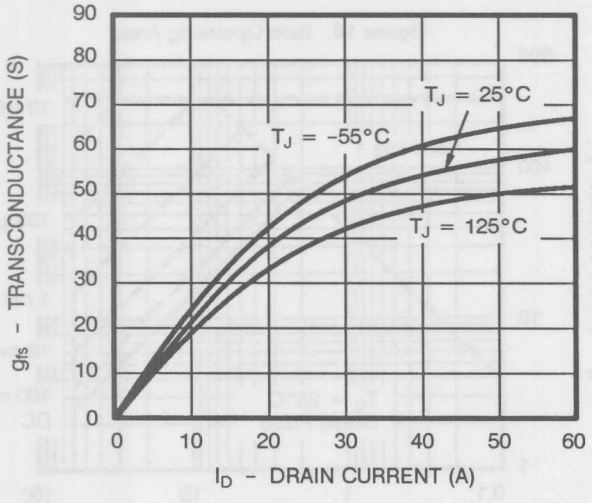


Figure 4. On-Resistance

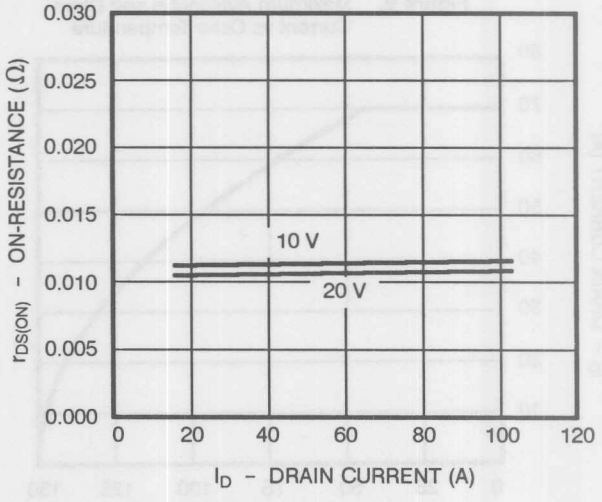


Figure 5. Capacitance

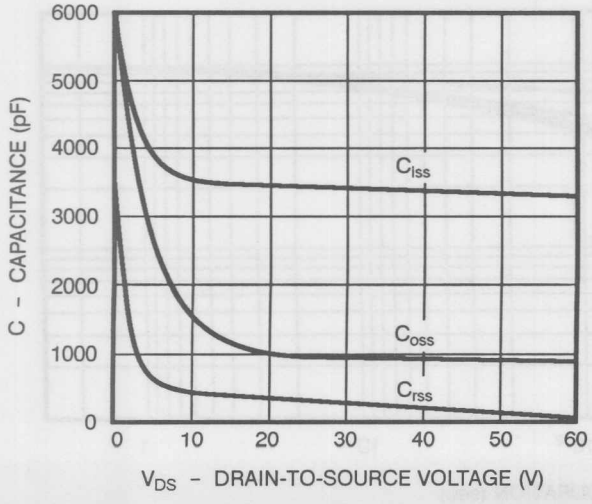
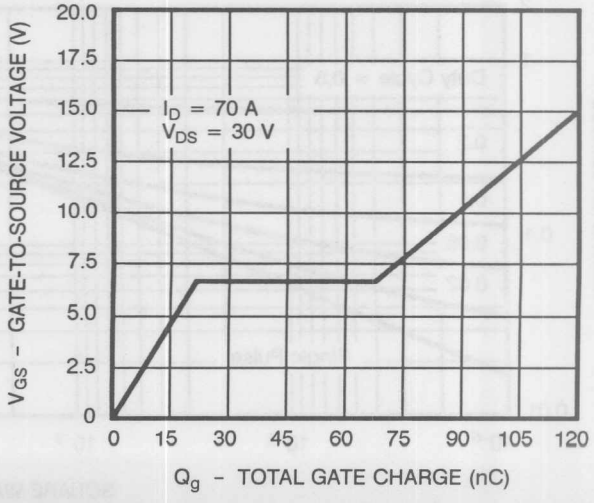


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

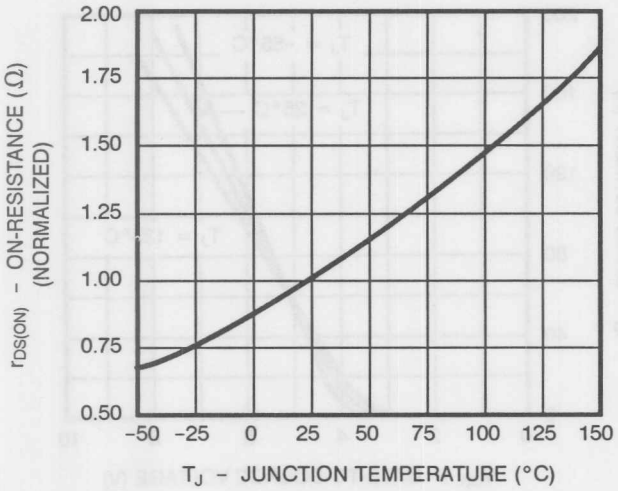
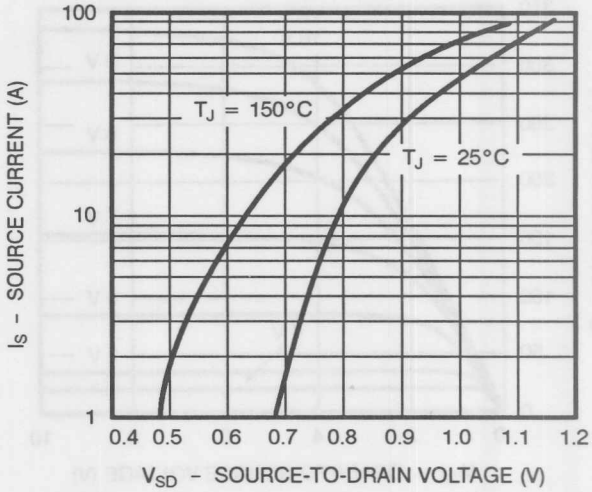


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs.Case Temperature

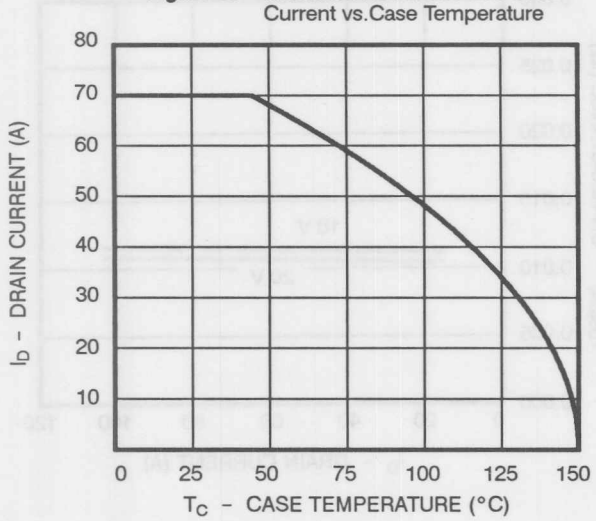
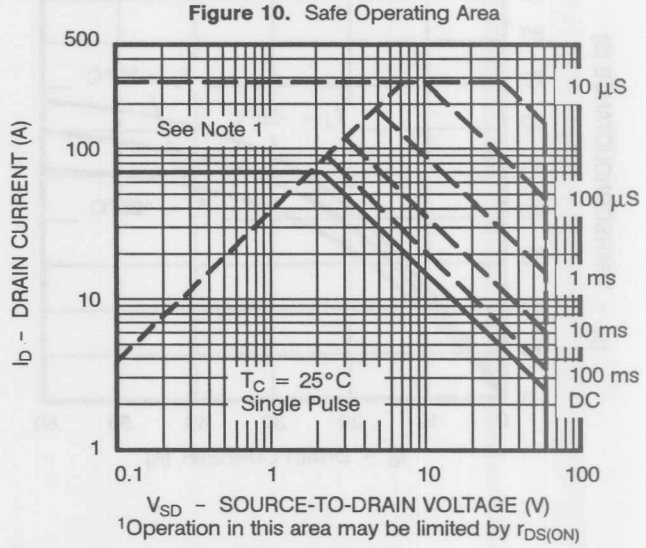
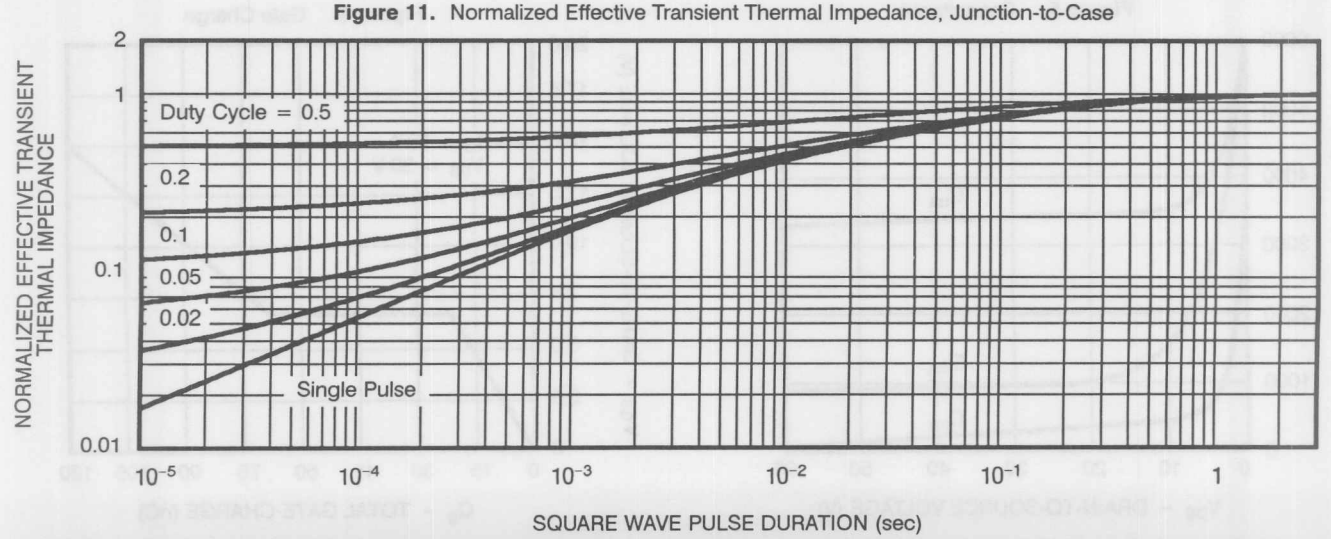


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(ON)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix SiMOS 2.5 Technology

A proprietary state-of-the-art MOSFET design called SiMOS 2.5 allows Siliconix to produce power MOSFETs with record-low on-resistance.

The name, SiMOS 2.5, is derived from the fact that the design consists of 2.5 million MOSFET cells per square inch of silicon — thousands of these MOSFET cells are in parallel on each chip. To pack 2.5 million MOSFET cells into a square inch of silicon, the physical size of each cell had to be made very small. Figure 1 shows a photograph of a die that was made using this technology. The individual cells are just visible as small squares on the die.

The SMP60N06-14 and SMW70N06-14 feature a rated drain-source resistance ($r_{DS(on)}$) of just 14 milliohms. While this resistance can be split into three components — the channel resistance, the JFET region resistance, and the EPI resistance — fifty to sixty percent of the total on-resistance of a typical 60-V MOSFET is attributable to the channel resistance. The current path and the three components of the $r_{DS(on)}$ are shown in Figure 2.

SiMOS 2.5 was designed to reduce the total resistance by reducing the channel resistance. The use of many small cells in parallel maximizes the total cell periphery on the MOSFET chip; therefore, channel resistance is dramatically reduced. The effect of density (or number of cells per square inch) on $r_{DS(on)}$ is shown in Figure 3. The high cell density used in SiMOS 2.5 gives a specific on-resistance (the resistance of a chip that is one centimeter by one centimeter) of 1.5 to 1.65 milliohms cm^2 at a 60-V drain-source rating. This low specific on-resistance allows Siliconix to manufacture a 14-mΩ chip small enough to fit in a TO-220 package.

Breakdown voltage is another factor that affects the $r_{DS(on)}$ of a MOSFET. Both the SMP60N06-14 and SMW70N06-14 are rated at 60 V. Figure 3 shows the reduction in $r_{DS(on)}$ that could be obtained by manufacturing the parts to have 50-V ratings — a technique used by some manufacturers to reduce

Figure 1.

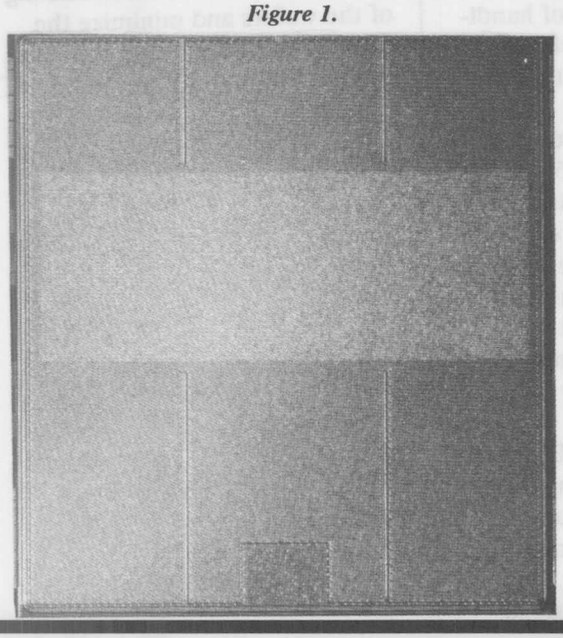
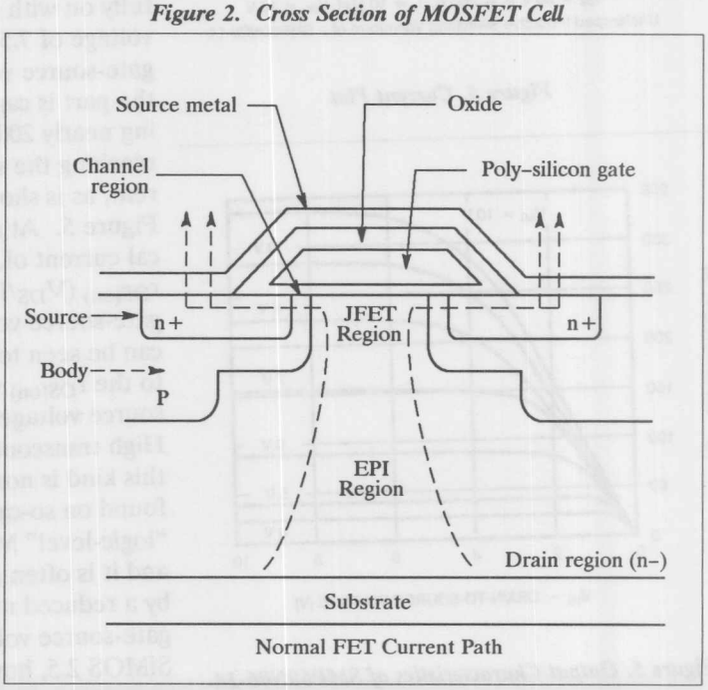
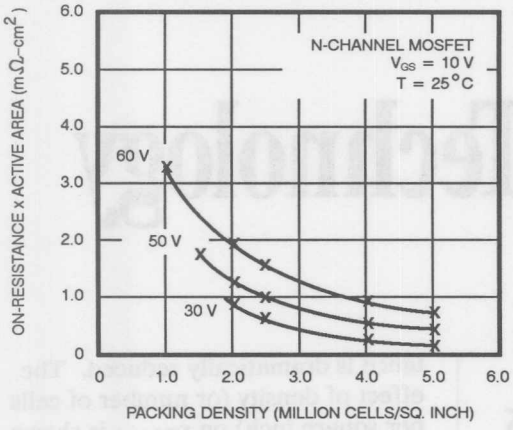


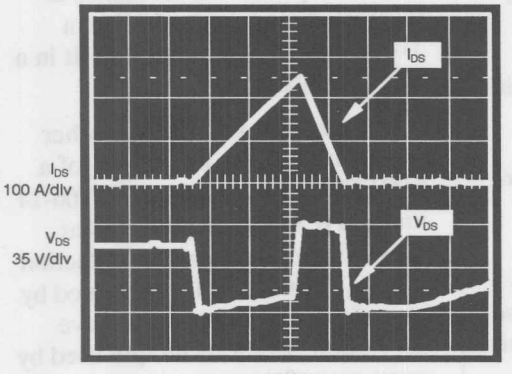
Figure 2. Cross Section of MOSFET Cell





Specific resistances of the 30-, 50- and 60-V n-MOSFET as a function of the packing density.

Figure 3. Cell Packing Density



VDS = 50 V, ID = 260 A, L = 10 µH, VGS = 10 V
Unclamped Inductive Switching Waveform of a SMP60N06-14

Figure 4. Current Plot

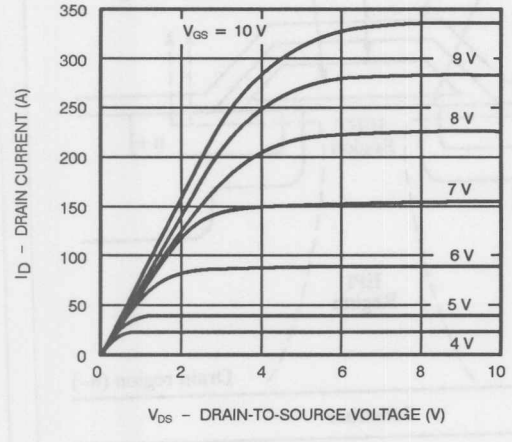


Figure 5. Output Characteristics of SMP60N06-14

$r_{DS(on)}$ ratings. With SiMOS 2.5 technology, a 50-V version of the SMP60N06-14 would be rated at less than 12 mΩ.

While much has been made of the low on-resistance achieved by SiMOS 2.5, the technology has produced several other noteworthy advantages: ruggedness, very high transconductance, and low gate-charge x $r_{DS(on)}$ product.

SiMOS 2.5, in fact, produces devices that set new standards for ruggedness—the ability of a power MOSFET to withstand high currents in avalanche. Figure 4 shows that an SMP60N06-14 can sustain over 250 A of current in unclamped inductive switching tests.

SiMOS 2.5, through the use of a proprietary gate oxide process, also improves the transconductance of the MOSFET. This means that although $r_{DS(on)}$ is rated at a gate-source voltage of 10 V, the part is essentially fully on with a gate-source voltage of 7.5 V. With a gate-source voltage of 7.5 V, the part is capable of handling nearly 200 A before reaching the saturation current, as is shown in Figure 5. At a more practical current of, say, 50 A, the $r_{DS(on)}$ (V_{DS}/I_D) with a gate-source voltage of 7.5 V can be seen to be very close to the $r_{DS(on)}$ with a gate-source voltage of 10 V. High transconductance of this kind is normally only found on so-called "logic-level" MOSFETs, and it is often accompanied by a reduced maximum gate-source voltage rating. SiMOS 2.5, however, accomplishes high-transconductance with a full ±20-V gate-source voltage rating.

The high cell density and proprietary gate oxide results in a very low gate charge x $r_{DS(on)}$ product, particularly if a gate-source voltage of 7.5 V is used. The SMP60N06-14 has a typical $r_{DS(on)}$ x Qg product of 1.1×10^{-12} coulomb ohms at a gate-source voltage of 10 V, and a product of 0.8×10^{12} coulomb ohm at a gate-source voltage of 7.5 V. This "figure of merit" is an indication of how much current the drive circuit will have to supply to charge and discharge the gate-source capacitance. The lower the product, the more simple the drive circuit will be. The low "normalized gate charge" produced by SiMOS 2.5 technology overcomes the problems encountered in driving, say, several 28-mΩ devices in parallel.

All SiMOS 2.5 die are manufactured in Siliconix' 6-inch wafer fabrication facility in Santa Clara, California. This facility, specifically designed to make high density power MOSFETs and power integrated circuits, contains less than one particle (0.2 µm and larger) per cubic foot, a cleanliness standard that can only be maintained by a high level of automation to reduce handling of the wafers and minimize the number of personnel in the clean room area. □